First Call for Papers

IEEE Asian Solid-State Circuits Conference (A-SSCC) 2007

Location: Ramada Plaza Hotel, Jeju Island, Korea
Date: November 12, 2007 (Monday) – November 14, 2007 (Wednesday)

Sponsored by IEEE SSCS, IEEE Region-10 SSCS Chapters

The IEEE A-SSCC 2007 (Asian Solid-State Circuits Conference) is an international forum for presenting the most updated and advanced chips and circuit designs in solid-state and semiconductor fields. The conference is supported by the IEEE Solid-State Circuits Society and will be held in Asia. Further details on the conference and paper submission guidelines and templates are available at the A-SSCC official website http://a-sscc.org/.

Paper Submission

Prospective authors are invited to submit full-length, four-page manuscripts, including figures, tables and references, to the official A-SSCC 2007 website. All papers will be handled and reviewed electronically. Papers are solicited in the following categories:

1. **Industry Program:** This special category accepts only papers based on state-of-the-art products. The paper may cover specifications, applications, state-of-the-art points, chip photos, chip architecture/software, circuits (not necessarily very original, significant improvement is fine), live demo if any, characterization results, and packaging/testing results.
2. **Analog and Data Conversion:** Analog circuits and subsystems, including baseband amplifiers, DC-DC converters, continuous-time & discrete-time filters, comparators, multipliers, voltage references, power-control circuits, non-linear analog circuits, op-amps, switched-capacitor circuits, Nyquist-rate and oversampling A/D and D/A converters, and sample-and-hold circuits.
3. **Digital Circuits and Systems:** Design, fabrication, and test of digital VLSI systems; microprocessors, network processors and chipsets; I/O and inter-chip communication; intra-chip communication; reconfigurable logic-array circuits; digital clock-synthesis circuits and architectures; high-performance and lowpower logic-micro-architectures and circuit techniques; high-speed digital circuits; power-reduction and management methods for digital VLSI, and implementation methodologies for digital VLSI.
4. **Emerging Technologies and Applications:** Advanced circuit technologies and techniques; ultra-low-voltage and sub-threshold logic design; molecular-, organic-, and nano-electronics; flexible substrates and printable electronics; 3D-integration and novel packaging technologies; compound-semiconductor, superconductive, and micro-photonic technologies and circuits; energy sources and energy harvesting; emerging applications such as biomedical and ambient-intelligence; emerging wireless applications and circuits; 3D RF and mixed-signal circuits; RFID; advanced signal-processing and microprocessor architectures; design for manufacturability; analog and optical processors, non-transistor-based analog and digital circuits and their system architectures; advanced memory technologies; spintronics; and quantum storage.
5. **Memory:** Static, dynamic, non-volatile, and read-only memory; circuit-design techniques, system architectures, I/O interfaces, and array organizations; magnetic and ferro-electric memory designs and architectures; data storage and multi-bit-cell-based memory designs; embedded memory architectures, cache-memory systems, multi-port memory, and CAM designs; emerging memory technologies; nano-crystal, phase-change, and 3D memories; high-speed low-power and low-voltage memory designs; yield-enhancement redundancy and ECC techniques; and memory testing and built-in self-test.
6. **Mixed Signal Processing:** Mixed signal-processing circuits and systems, digital signal processors and systems, reconfigurable signal-processing circuits and systems; low-power signal-processing circuits and systems; baseband-communication-processing architectures; cryptographic- and security-processing circuits and systems; magnetic and optical storage circuits and systems; multimedia processors and systems, image-processing/compression architectures, audio-and-voice- processing/compression architectures, bio-medical/neural signal processors.
7. **RF:** Circuits and sub-circuits for RF/IF/baseband, including receiver and transmitter front-end circuits; narrowband RF; ultra-wideband and millimeter-wave circuits (MMDS, 60GHz); IF amplifiers; power amplifiers; RF switches; power detectors; active antennas – including MIMO, modulators, and demodulators, synthesizers, and PLLs.
8. **Student Design Contest:** A student design contest is held among **the accepted papers** with system prototypes or measurement results of which operations can be demonstrated on-site. Refer to the web for further information.
9. **Wireless and Wireline:** Receivers/transmitters/transceivers for wireless systems including (but not limited to) WLAN, WPAN, WMAN, GPS, DVB/DMB, Bluetooth UWB, GSM/EDGE/CDMA/UMTS/3G/4G base stations and handsets, TV/radio/satellite; receivers/transmitters/transceivers for wireline systems including (but not limited to) LAN, WAN, FDDI, Ethernet, token-ring, fiber channel, SONET, SDH, PON, ATM, ISDN, xDSL, cable-modem; optical/electrical data links and backplane transceivers, power-line/phone-line home networks, subscriber-line circuits and modems. Wireline transceiver building blocks like AGC, oscillators, line-drivers and hybrids.

The papers on low-power and/or low-voltage approaches, signal integrity, noise, test, and manufacturability for all the above categories are welcomed. Measurement results are highly recommended, especially for analog, and RF categories. Design methodologies for SiP, SoC, interconnections and statistical design are included in the scope of the conference; the papers only describing CAD tools and CAD algorithms are not considered. Dual submission to other conferences is not allowed. A special issue of the IEEE Journal of Solid-State Circuits will be prepared for publication of the outstanding papers of this conference.

Important dates

June 11, 2007, 20:00 (GMT)	Paper submission deadline
July 31, 2007	Acceptance notification
September 1, 2007	Deadline for final papers submission

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