How to write a good **Journal of Solid State Circuits** paper

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[A-SSCC 2008, Fukuoka, Japan]

Outline

- **About the Journal**
  - Yesterday and today
  - Journal versus Conference
  - Organization of the Journal
  - What kind of papers?
- **Writing tips**
  - Paper outline
  - General tips
- **How NOT to write a JSSC paper**

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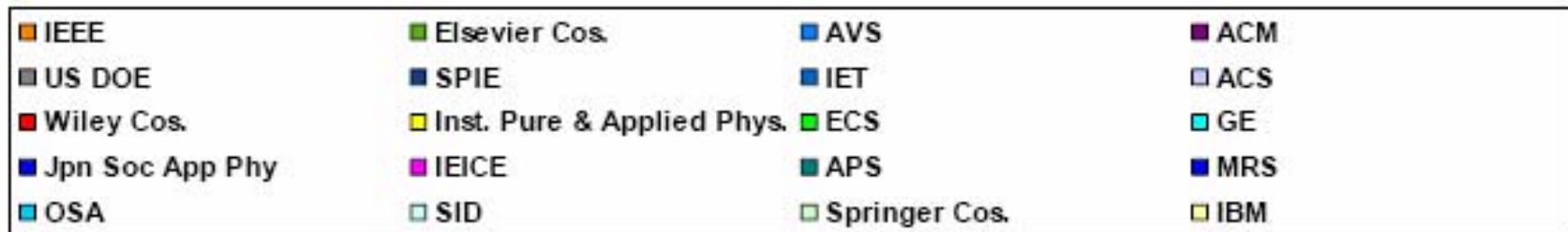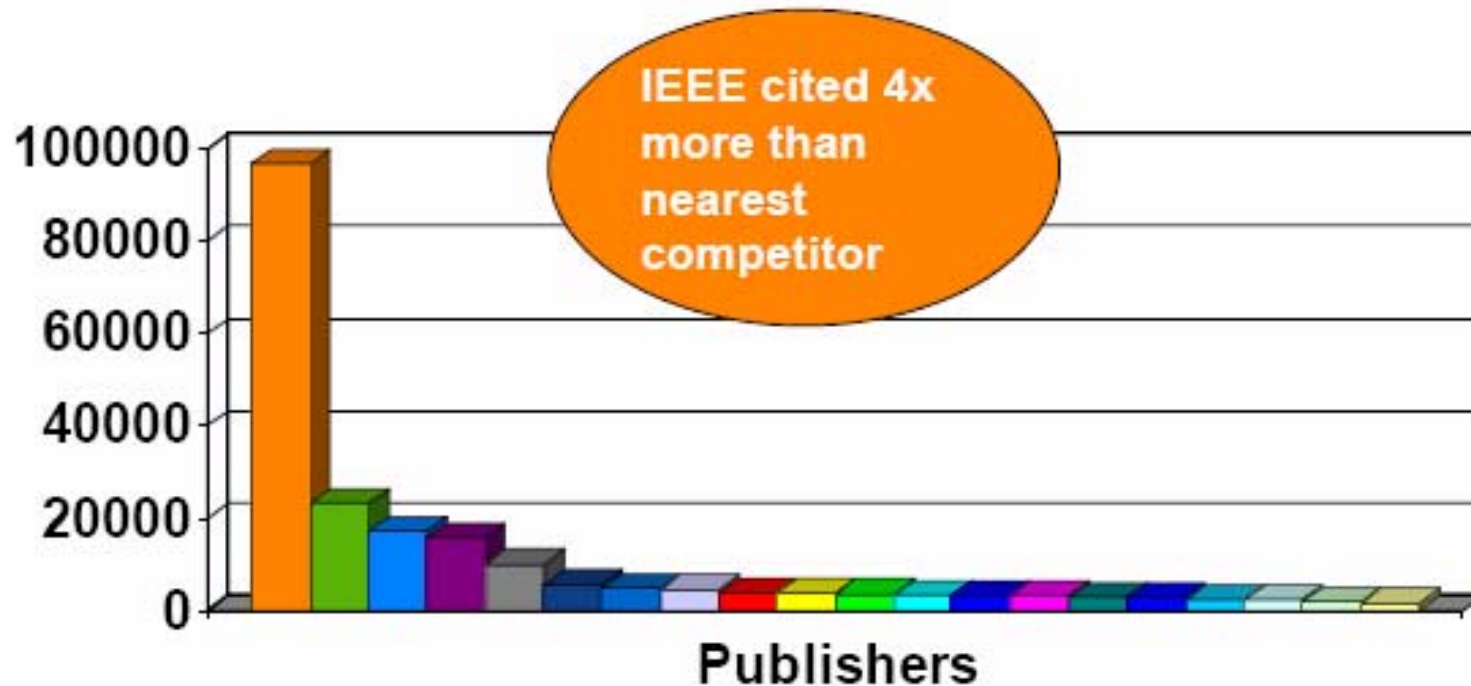- How NOT to write a JSSC paper

History

- Established in 1966
  - 4 issues per year
- Volume 1, nr 1: ISSCC 1966 issue

- Purpose= archive

TODAY

- ***The*** Nr 1 IEEE Journal
- By far: most downloaded IEEE Journal
- By far: most cited in all US Patents
  - Over all technical disciplines

References in patents from top 25 companies to top 20 publishers

Top cited IEEE Journals in patents

Rank	Title	Cites
1	**IEEE Journal of Solid-State Circuits**	**14,765**
2	IEEE Transactions on Electron Devices	8,824
3	IEEE Transactions on Communications	8,678
4	IEEE Photonics Technology Letters	8,383
5	Journal of Lightwave Technology	5,989
6	Proceedings of the IEEE	5,338
7	IEEE Transactions on Magnetics	5,071
8	IEEE Transactions on Computing	4,393
9	IEEE J on Selected Areas in Communications	4,148

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Conferences

- Fast publication
- Usually a smaller idea
  - Benchmark: Known circuit in new technology
  - Smaller trick can be o.k.
  - depends on conference
- Just accept or reject; no rewrite
  - It may be incomplete
  - It may lack key references
- Good for networking and Q&A
- Widely available on IEEExplore

Journal publication

- Academic reputation
  - Journals have ~4x more status than conferences
- Reviewed Journal gives a "quality stamp"
  - Reviewers demand corrections & clarifications
- Archive your work
  - Wider scope
  - More theory
  - More technical information
  - More Educational
  - More references

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Organization regular JSSC papers
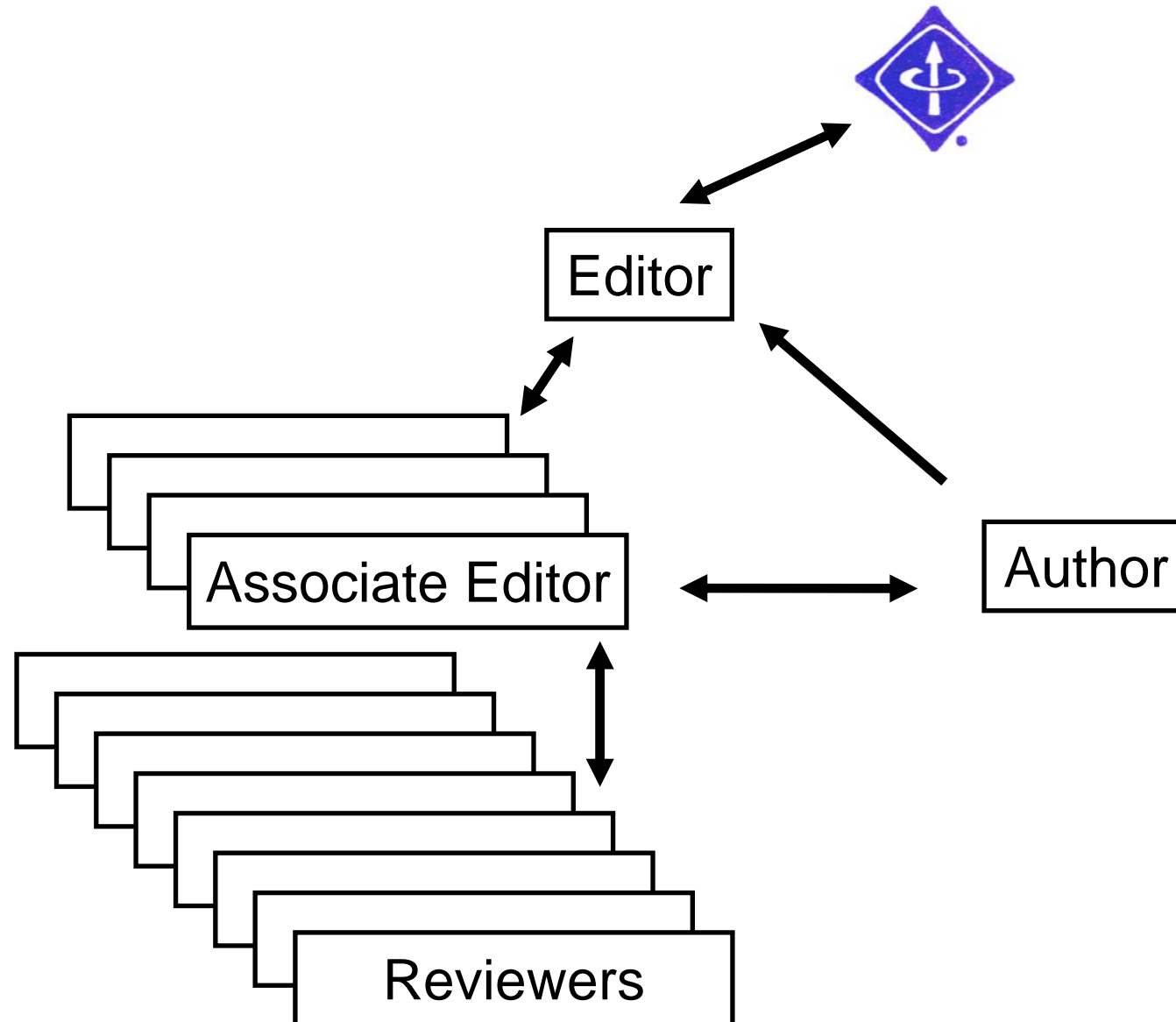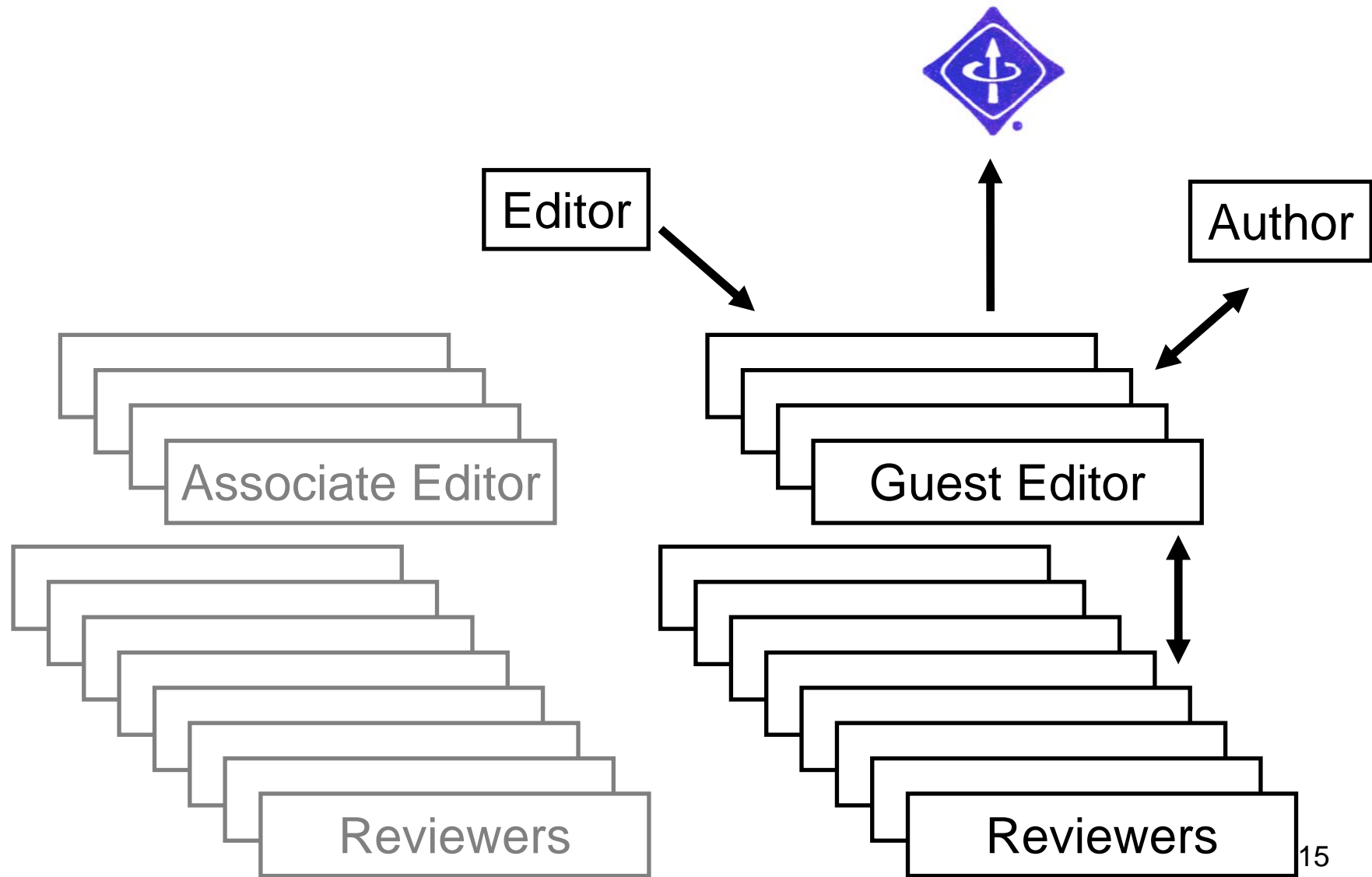
Associate Editors

- **Baas**, Bevan
- **Behzad**, Arya
- **Flynn**, Michael
- **Gharpurey**, Ranjit
- **Gillingham**, Peter
- **Halonen,** Kari
- **Karanicolas**, Andrew
- **Kim**, Beomsup,
- **Leenaerts**, Domine
- **Liu**, Shen-Iuan,

Mok, Philip
Nairn David
Natarajan Shreedhar
Rusu, Stefan
Razavi, Behzad,
Savoj, Jafar
Shaeffer, Derek
Shepard, ken
Young, Darrin

Special Issues on conferences

- December   ISSCC-analog, RF   (issue)
- January   ISSCC-dig+rest   (issue)
- April   VLSI   (issue)
- May   RFIC   (section)
- July   ESSCIRC   (issue)
- August   CICC   (issue)
- September   BCTM   (section)
- October   CSIC   (section)
- November   A-SSC   (section)

Organization special Issue

Editor → Associate Editor (stack)

Guest Editor (stack) → Author

Reviewers (stack)

Reviewers (stack)

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Procedure (regular papers)

- Author submits manuscript to Editor
- Editor sends to Associate editor
- Associate Editor sends to reviewers
- Associate Editor makes decision:
  - AWR   accept with revisions ☺
  - REJ   reject
  - REF   refer to other Journal

  Its not a democratic process!!!!!!!!!!!

Procedure (regular papers)

- Author rewrites
  - Give list of how you changed manuscript based on reviewers comments
  - Do not reply to reviewer but change your manuscript
- Associate Editor makes final decision
- OR: Associate Editor organizes second review

- Author submits final package to Associate Editor
- Associate Editor inspects and forwards to Editor
- Editor compiles issues and sends to IEEE

Time schedule (regular papers)

- Delay to first decision   ~100 days
- Delay author rewrite   ~100 days
- Publication delay   ~140 days

- Total delay   ~340 days

Origin of regular papers

- 365 submissions/year: 1/day
  - Asia   40% (Taiwanese Universities)
  - USA   25%
  - EU   25%
  - ROW 10%

- Same regional distribution as ISSCC
- 90% is analog/RF!!

Accept/reject regular papers

- Accept   36%
- Reject   58%
- Refer to other Journal   3%
- Withdrawn   3%

- Main reject reasons:
  - Not enough **novelty/innovation**
  - Not enough news w.r.t. **prepublication**

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What papers are good for JSSC?

- IC Implementation oriented
  - Not: microwave PCP/ modeling/ device only
- Not too much theory (Better use TCAS)
- Integrated Circuit needed
- But to have an IC is not enough!

The work must be of HIGH Quality

What is high quality?

- Must describe an **INNOVATIVE IDEA**
  - Not just a permutation
  - Not a know circuit in new technology
  - Not a combination of known techniques
  - But a real new concept / invention
- AND idea must be proven on IC
- AND idea must significantly advance state-of- art

Prepublication

- ~90% of submitted papers have prepublication at conference(s)
  - That's ok

- Conferences are available on IEEExplore

- So a JSSCC paper should add significant information to the prepublications

Prepublication policy

- *"A JSSCC paper should be worth reading for a person who has read the conference paper."*
  - Better description of state-of-art
  - More theory + proof of concept
  - More measurements
  - More discussion (mismatch, no-idealities etc)
  - More benchmark, more discussion
  - More references

Prepublication policy

- NOT each conference paper deserves to be a JSSC paper

- NOR each work without prepublication deserves to be a JSSC paper

- It's a delicate thing, but all about **QUALITY**

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A Typical paper outline

- Title
- Abstract
- Introduction
- Body
- Experimental results
- Discussion
- Conclusion
- references

The Title

- Must describe the paper
- Not too vague
  - "A novel receiver"
    - Do not use *"novel"* anyway
  - "5-GHz RF Frontends for Ultra-Low-Voltage and Ultra-Low-Power Operations"
    - How much is is Ultra?
- But exactly what is really new:
  - "Noise canceling technique for wideband receivers"
- Or exactly what is achieved
  - "A 1.5GHz 1.3dB NF, 10mW down converter in 65nm CMOS for GPS applications"
- Or both!

Abstract

- 1 paragraph
- Exactly what paper is about
- Can have overlap with conclusions
- Keywords, indexing terms
  - Use many!!
  - So your paper can be found
  - You will be cited a lot

Introduction

- Describe the problem you solve
  - Open the subject
  - Zoom in step by step
  - Describe your assumptions
  - Each step is one paragraph
- Describe the state-of-art
  - Use plenty of references
- Tell basic your idea
  - This motivates the reader to continue
  - Cite your prepublications and tell the difference
- Give outline

The body

- Explain your key idea

- Build up Step by step
  - One thinking step at the time
  - Each step is one paragraph

- Proof it makes sense
  - Use mathematics
  - Give exactly your boundary conditions
  - Give results in comprehensive way

The body

- Be self-critical and realistic:
  - does it really make sense?
- E.g. for a linearity improvement technique:
  - If power dissipation is larger
  - And noise is also larger
  - And you know that P~SNR: does this make sense?
- Is it just the technology or your smartness?
  - E.g. speed ~f_T or f_{max}
- Are practical boundary conditions met?
  - VCO @ high frequency but Pout=-30dBm

Experimental Results

- Describe exactly what has been measured and how.
  - Describe setup
  - "Bio Biased"?
  - Probe or PCB?
  - What equipment?
  - How many samples?
  - PVT?
  - Batch to batch spread?

- Experiment must be repeatable and of practical use for industry.

Experimental Results

- Compare with theory / simulations
- Does it prove your idea and theory?
- Always tell if a result is measures. Simulated or calculated.

"Figure x shows the noisefigure versus frequency"

➡ is this measured? Simulated? Calculated? Estimated?

IC realization

- Give chip photograph
  - Dimensions
  - What is what
- Give technology + options

Discuss results

- Compare to state-of-art in fair way
  - Show all relevant data + papers
  - Use table

- Use common FoM definitions
  - ADC, VCO, filter

- Be careful to define your own FoM
  - Do not misuse FoM for showing off
  - Power ~ SNR. BW makes sense
  - Power/bondpad is NOT a good FoM!!

Discuss results

- Help the reader to interpret the results
- Absolute accuracy needed?
    - show many samples, proof batch to batch robustness
- Matching needed?
    - show many samples
- Calibrated circuits?
    - describe what input signal is used/required. When does it go wrong? How realistic is it?

Discuss Results:

A useless PLL benchmark:

Specifications	Unit	This Work	[6]	[13]
Technology	—	0.18-μm CMOS	0.18-μm CMOS	0.25-μm SiGe BiCMOS
Frequency	GHz	10.3	10.0	10.0
Supply Voltage	V	1.8	1.8	3.3
Power Consumption	mW	113	—	—
Locking Range	GHz	10.1 ~ 11	—	—
Peak-to-Peak Jitter	ps	3.72	6.5	4.8
RMS Jitter	ps	0.43	0.6	0.4

Conclusions

- Start writing with this
- First make a bullet list for yourself
  - A hand full of bullets
  - So you know where to write towards
  - This gives your paper focus
- Conclusion should be readable without reading the whole paper
- Convince the reader

What did we learn?

References

- Include latest state of the art
  - For benchmark
- But also refer to the original papers
  - Go back in time!
  - Most references are younger than 5 years ☹
  - While most ideas are much older!
- Textbooks are useful too

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Writing tips:

A well written paper gives the impression of a good idea

Writing Tips

- If a paper is too complex:
  - Reviewers don't understand it
  - Reviewers don't believe it
  - Reviewers will not like it

- If a paper is too simplistic
  - Reviewers think its nothing special
  - Even if the results are good

General writing tips

- Make your problem relevant
- Start with the "big picture"
- Take the reader by the hand
  - Step by step explanation
- Highlight innovation
- Do not give too many equations
- Do not give too much theoretical details
- Do not try to make a tutorial

General writing tips

- Do not use "very" but give the numbers
- Avoid to use "novel"
  - everything you don´t cite should be novel
- Use short sentences
- Use simple words
- One point per paragraph
  - First or last sentence is most important
  - The rest is explanation
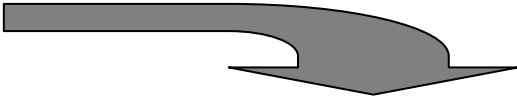
General writing tips

- If you are stuck:
  - Tell a friend what you did.
  - Use the words & slides like on your conference paper
  - Polish the text later
- Let a fellow student read & comment
- Ask native speaker to correct language
- Polish, Polish, Polish
  - Reviewers hate mistakes!!
  - It iz raely anojing to raed tekst width misstakes

Figures

- Make the figures like a cartoon
  - Reader can understand idea by looking at figures + caption only

- Spend a lot of time to make good figures
  - Papers with bad figures almost always get rejected

Figures

- Must be readable in single column:
- Not good:
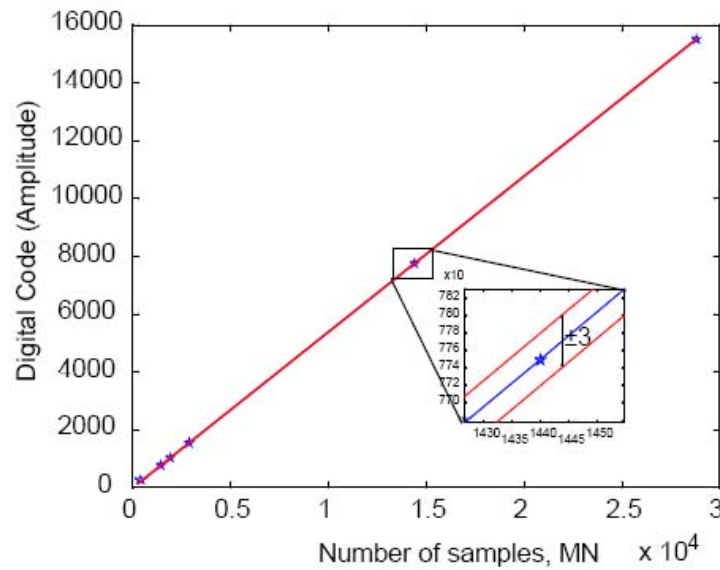
a)
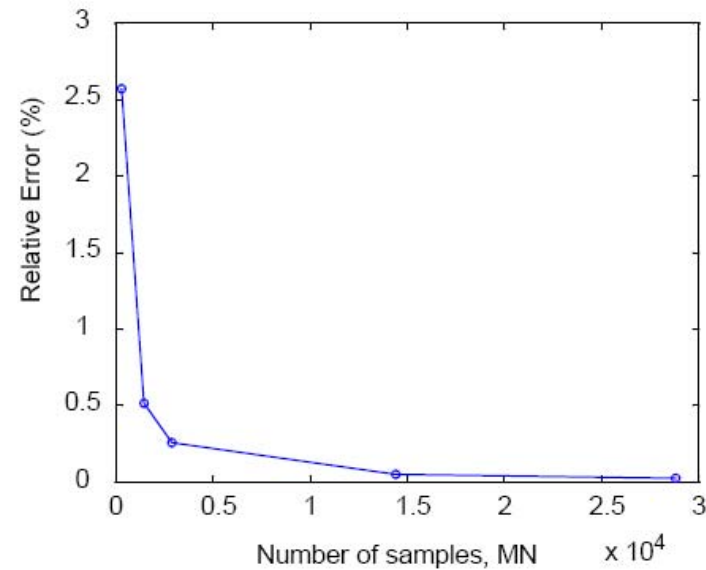
b)

Figure 13

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Do NOT

- Publish the same material elsewhere
  - Reviewers+readers always see this; its unethical
- Change your paper after acceptance and before publication
  - E.g. remove reference to competitor
  - Reviewers always see this
- Use someone else´s ideas
  - "Someone else" is reading too
- Hide "unpleasant" measurements

Do NOT

- Fabricate or falsify results
  - Not tune bias for each measuring point
  - Not make few chips and measure different parameters on different chips
  - Or even completely falsify papers (!)

Some falsification issues

If you publish good results which are falsified

Then other engineers will try to use your idea

And find out it cannot work!

(and this is NOT good for YOUR career!!!)

Author x, CMOS circuit 1, Journal of Solid-State Circuits
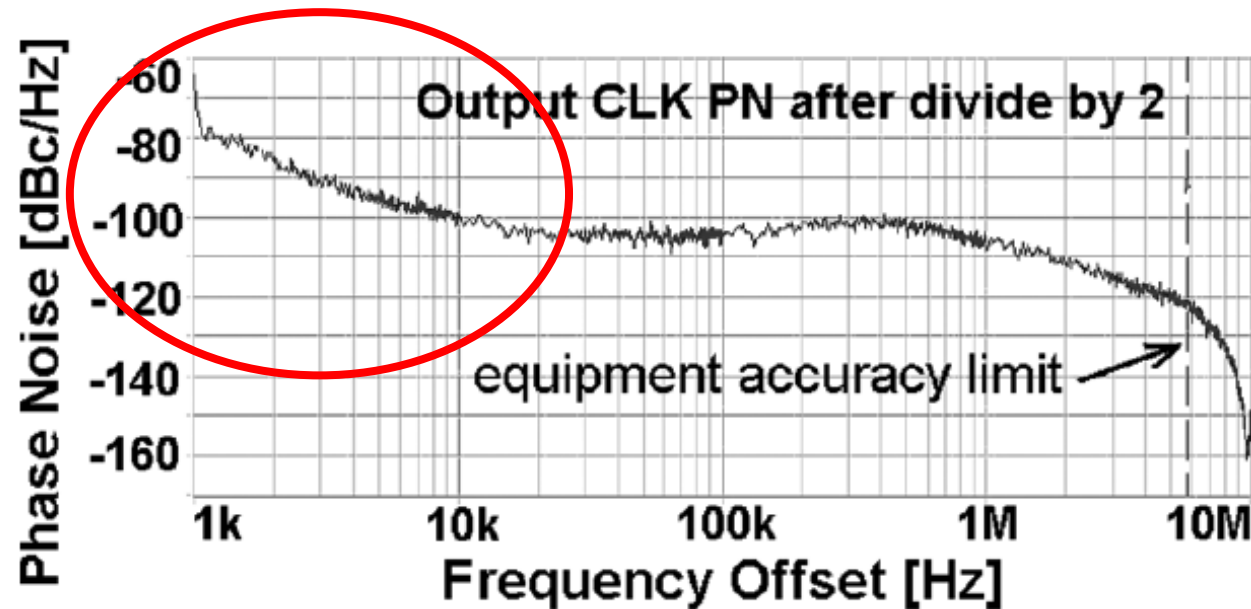
Fig. 16. Ring-VCO PLL closed-loop phase noise characteristic after additional divide-by-two (6 dB improvement).

Author x, BiCMOS circuit 2, Symposium y
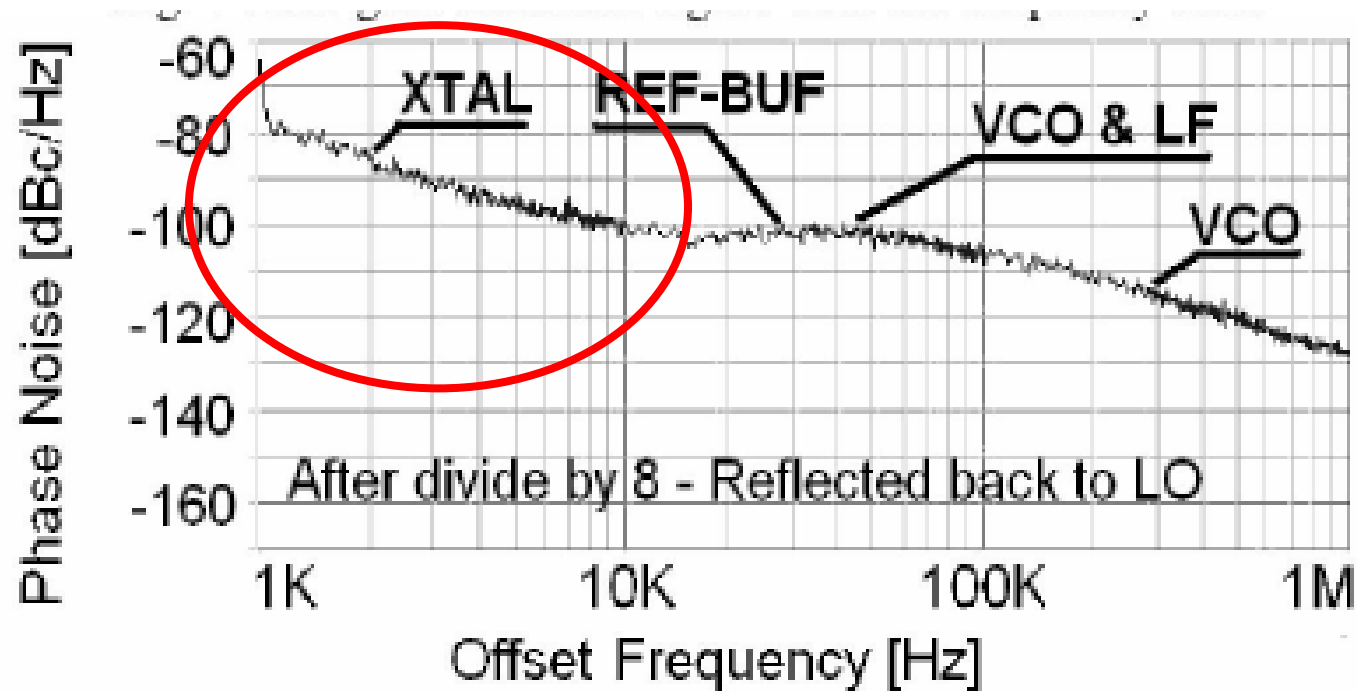
Fig. 8 LNB frequency synthesizer phase noise

2 Designs, 2 technologies same Phase noise!
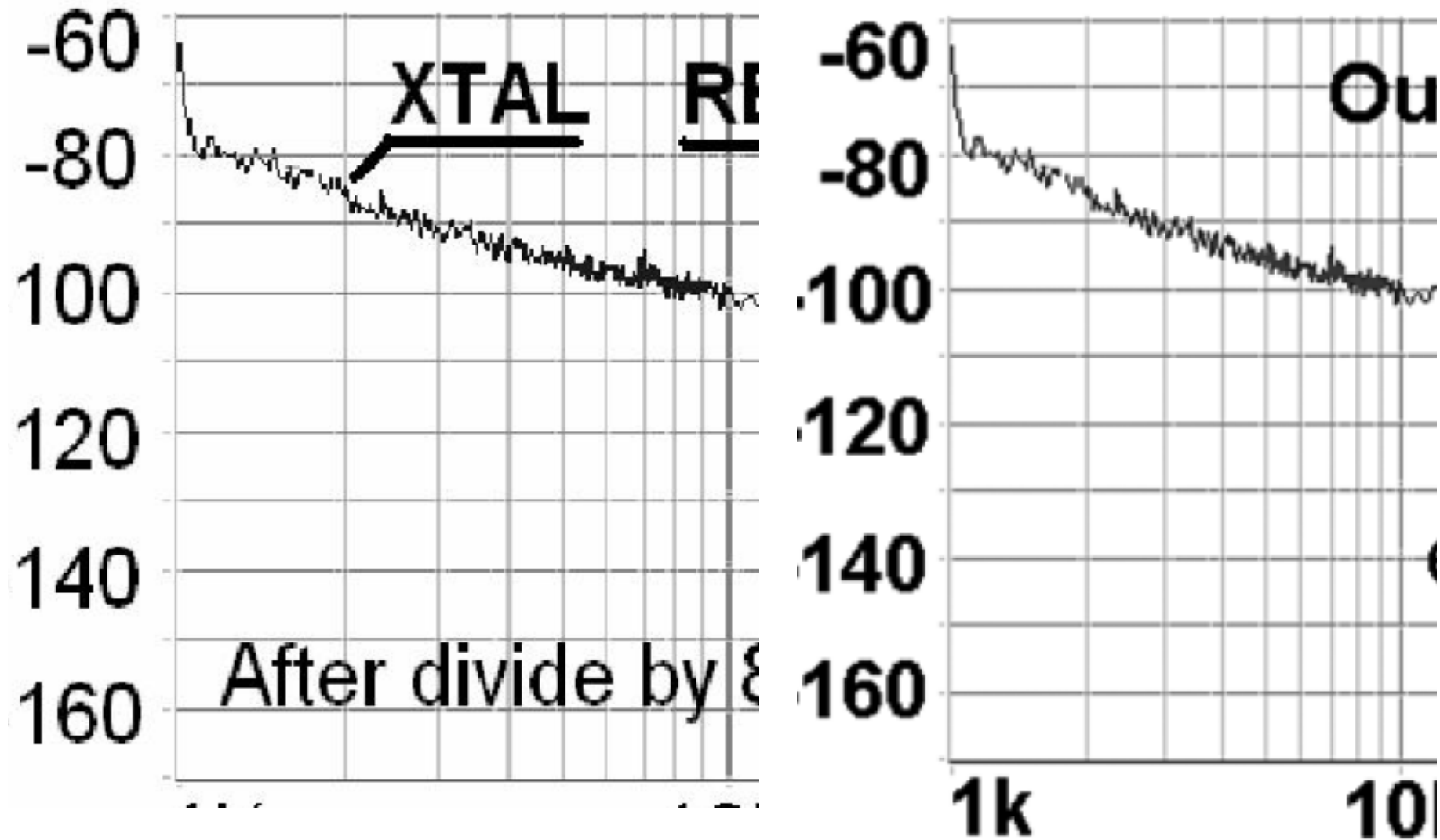
Author x, BiCMOS circuit 3, Journal of Solid-State Circuits
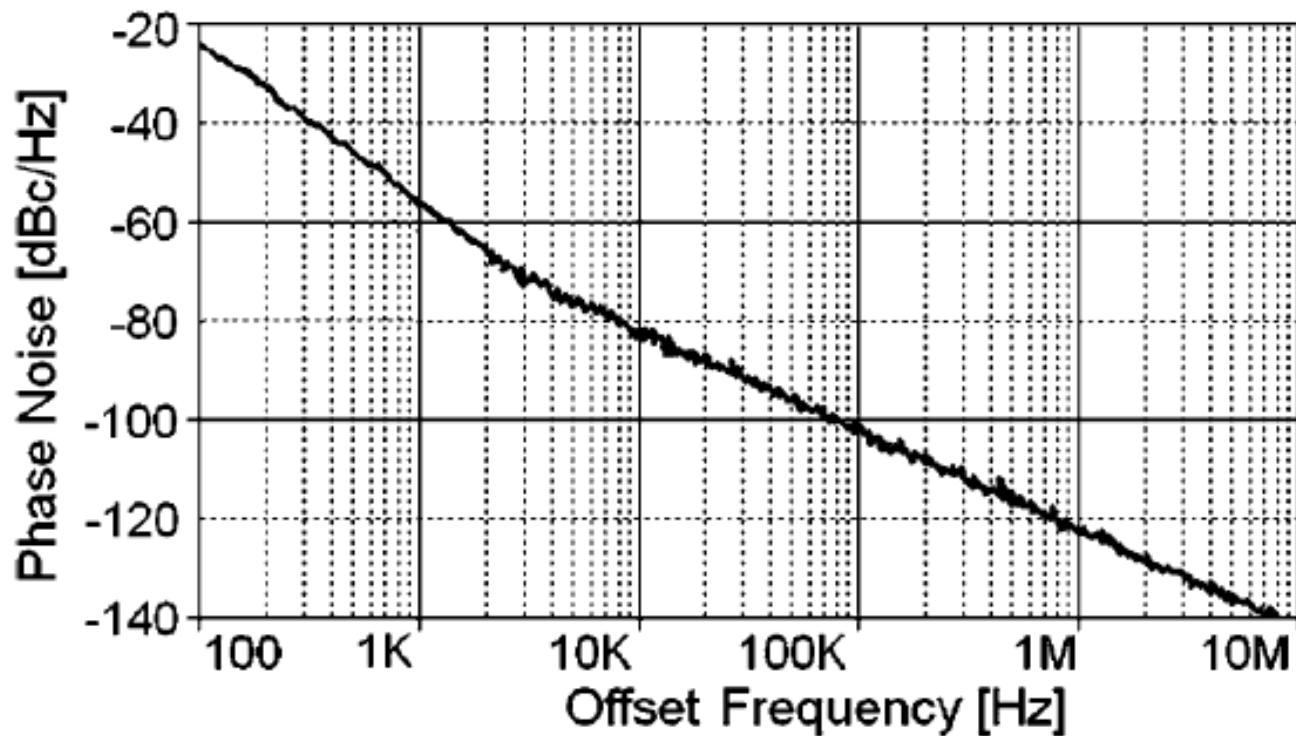
Fig. 12. VCO's output clock phase noise ($f = 9.953$ GHz, $V_{CC} = 3$ V, temperature $= 125\,^\circ$C).
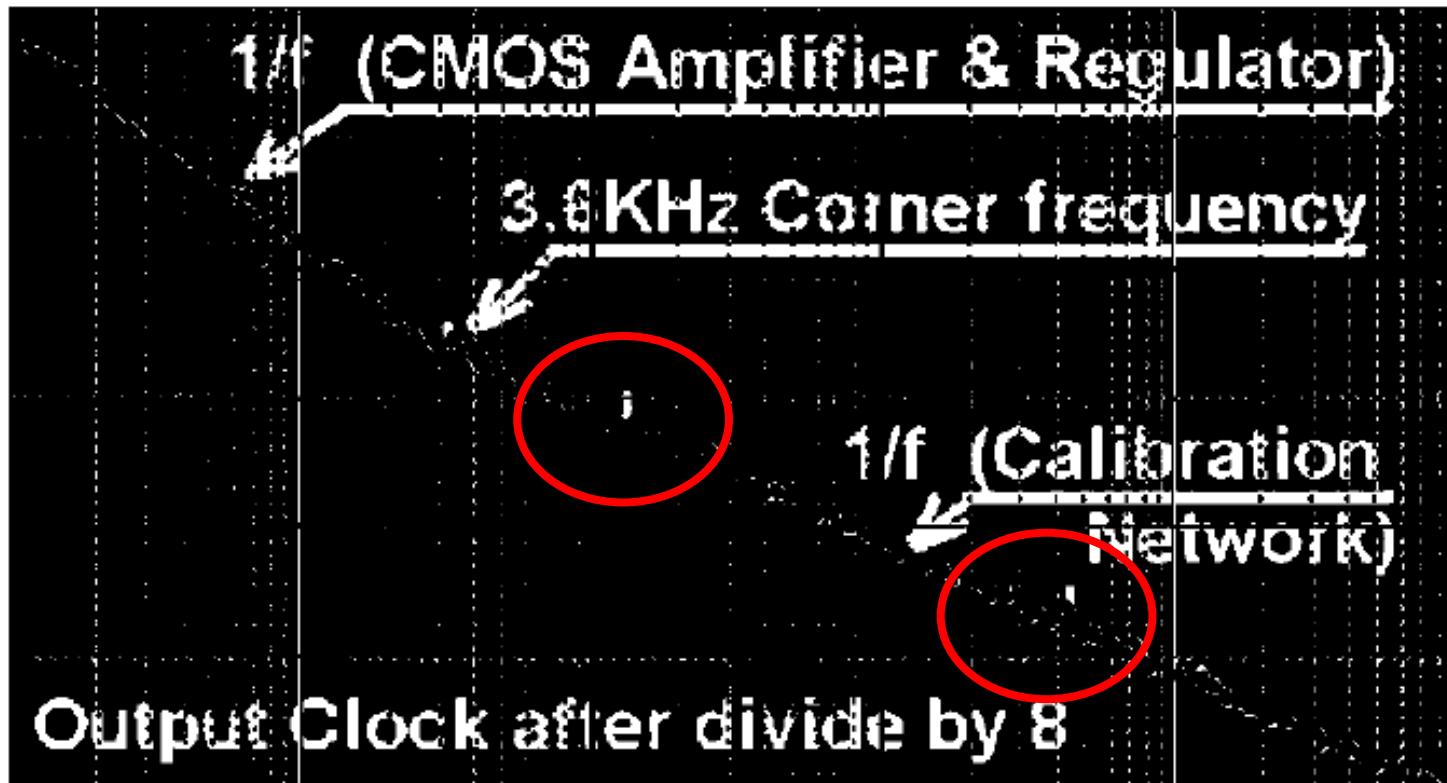
Author x, CMOS circuit 4, Symposium 2
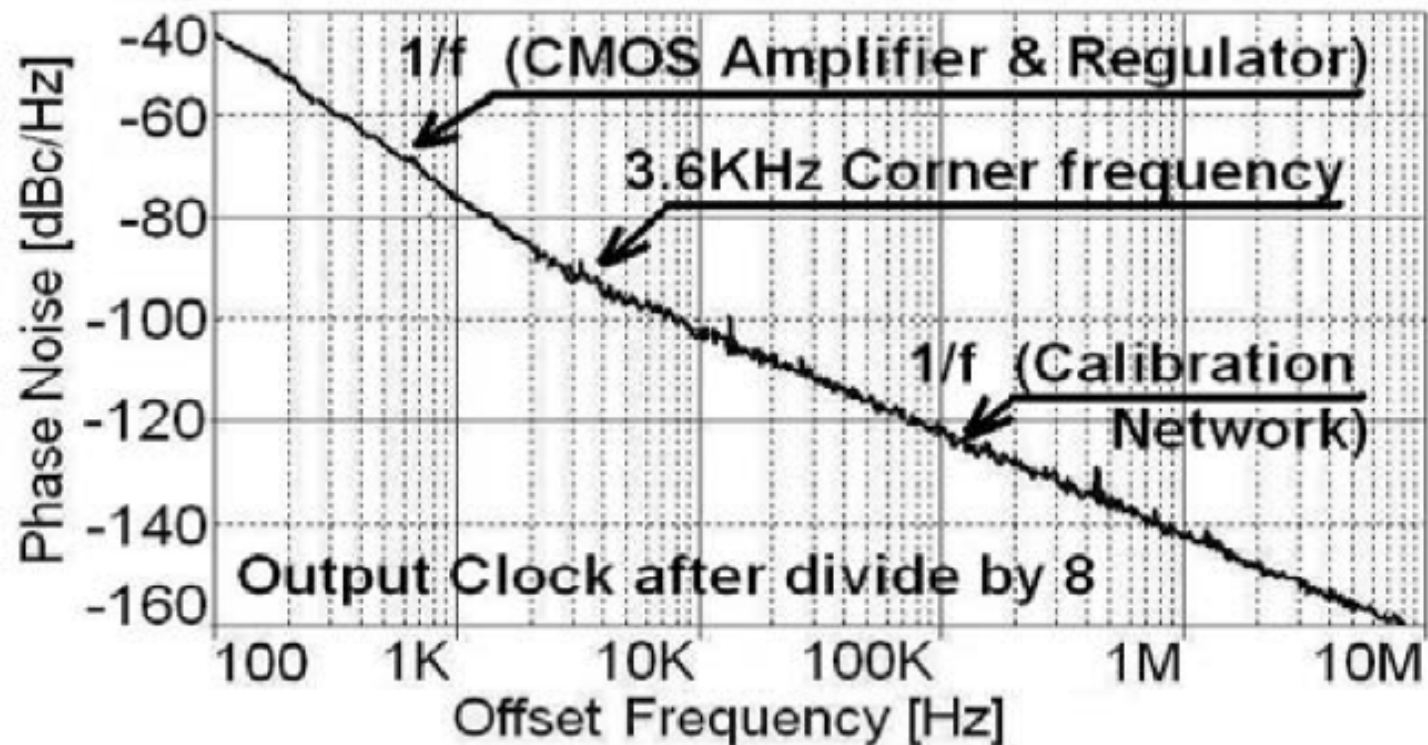
Fig.6 LC-VCO phase noise @ 10GHz, 125∘C, 3V

The Difference of 2 plots:
(2 spurs added)

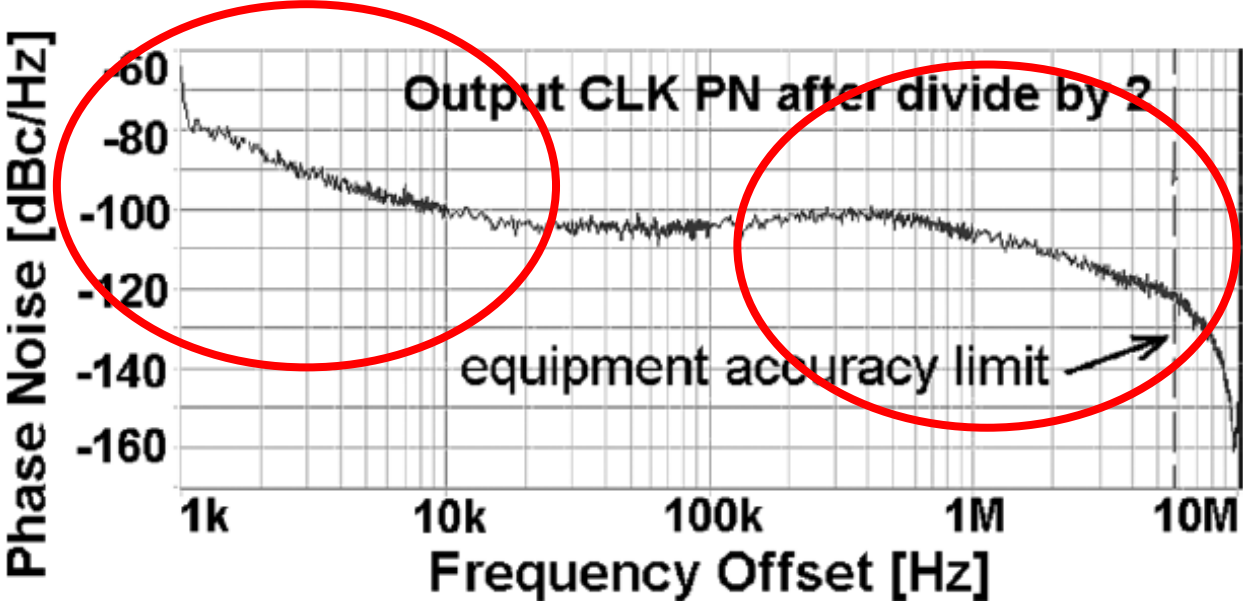**Author x, CMOS circuit 5, Journal of Solid-State Circuits**

Fig. 16. Ring-VCO PLL closed-loop phase noise characteristic after additional divide-by-two (6 dB improvement).
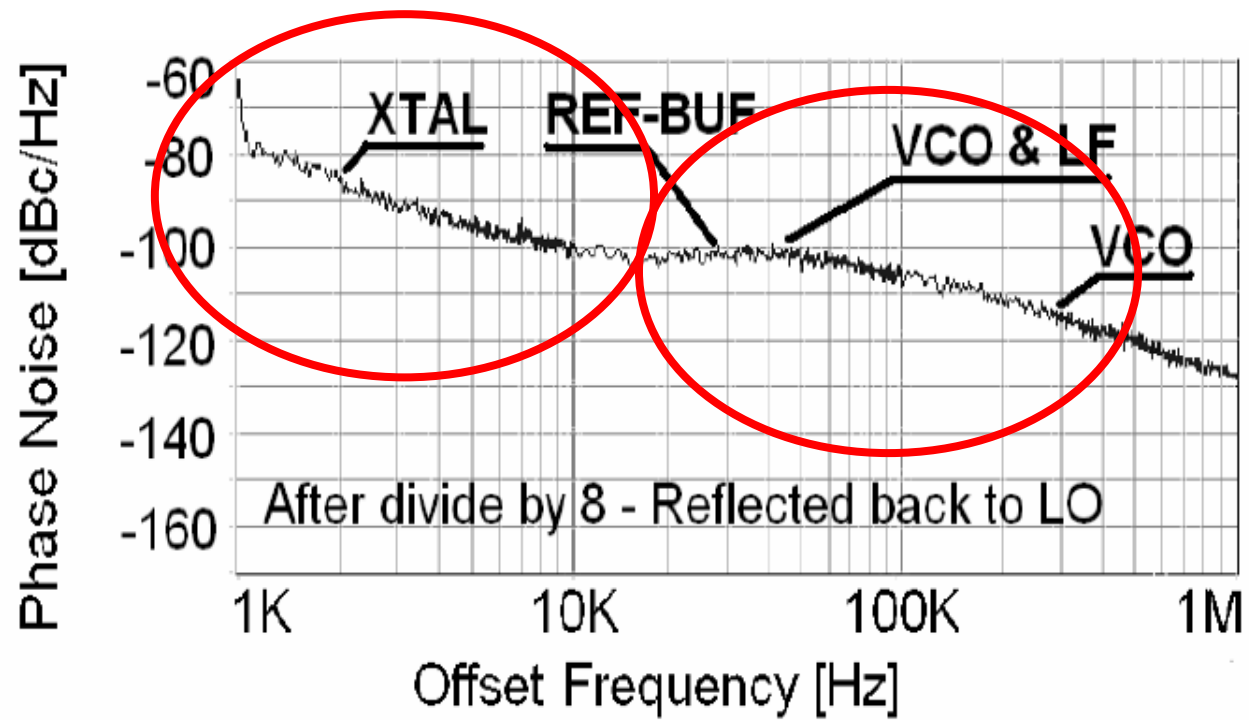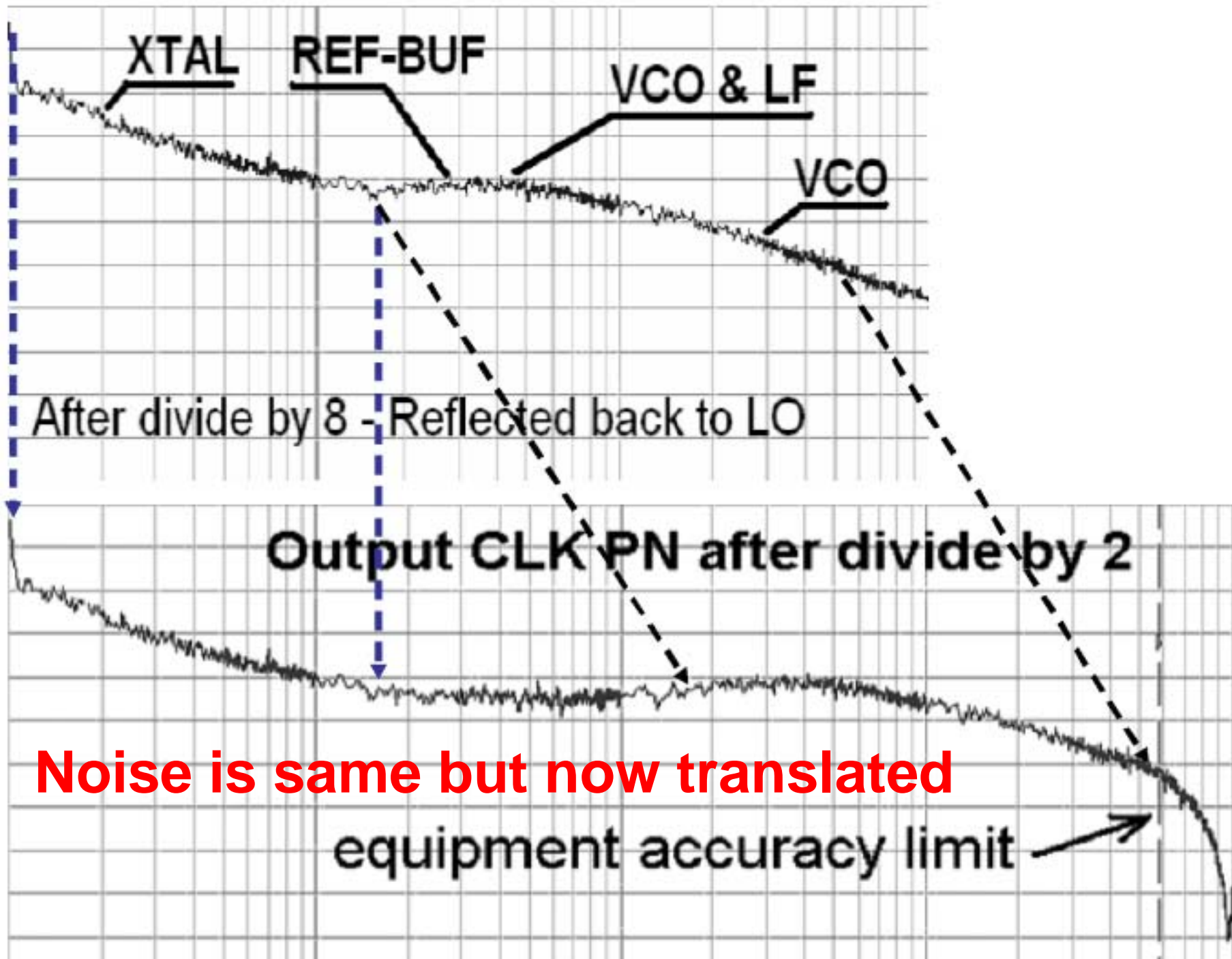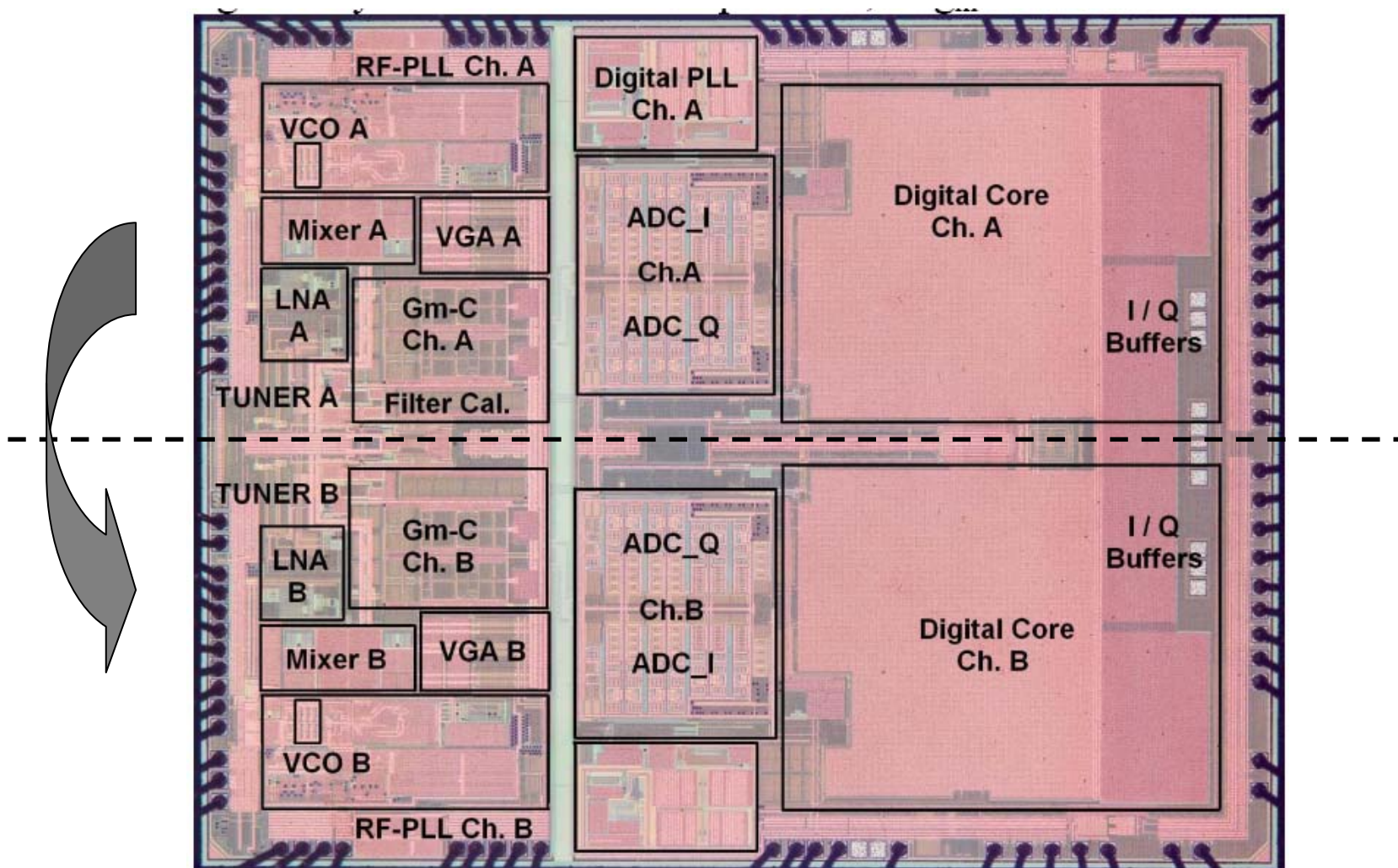
Author x, BiCMOS circuit 6, Symposium 3

Fig. 8 LNB frequency synthesizer phase noise

XTAL REF-BUF VCO & LF VCO

After divide by 8 - Reflected back to LO

Output CLK PN after divide by 2

Noise is same but now translated

equipment accuracy limit

Author x, CMOS circuit 7, Symposium 4

Photoshopped chip photo (flip over x-axis)
Also the dust is symmetric!!!

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Summary

- IEEE Journal of Solid-State Circuit
  - Most downloaded, most cited in patents
- Needs an Innovative new idea
  - Working silicon is not enough
  - Must improve state-of-art
- Needs new material after prepublication
- Reviewers are demanding
- Your writing technique can help