"Design of Femto-joule Energy Efficient ADCs in CMOS"

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In recent years significant energy efficiency improvements in A/D converters have been realized. Where a few years ago energy efficiencies of around 1pJ/conversion step were considered state-of-the-art, nowadays efficiencies down to fJ/conversion step are being reported.

In this tutorial the techniques and architectures used to reduce the power consumption of data converters designed in nanometer CMOS processes for wireless applications will be explained. The tutorial will first introduce the basics of A/D converters, their performance specifications and typical architectures. Next the techniques used to improve energy efficiency will be introduced and examples of implementations will be given. These include fully dynamically clocked flash type converters with offset compensation that enables 50fJ/step data conversion for a 5b 1.75GS/s data converter. The passive charge sharing SAR A/D technique with noise reduction by redundancy similarly improves the energy efficiency to 54 fJ/step for a 9b 40MS/s design. And finally, a two-step architecture employing the CABS principle, which is a new implementation of a successive approximation algorithm, improves the power efficiency to 10fJ/conversion step for a 7b 150MS/s converter.

All this will be explained in detail, with emphasis on design issues relevant for a successful implementation of the techniques.

Geert Van der Plas is Principal Scientist in the Wireless Research group of IMEC/NES. He obtained the M.Sc. and Ph.D. degrees from the Katholieke Universiteit Leuven, Belgium, in 1992 and 2001, respectively. From 1992 to 2001, he was a Research Assistant with the ESAT-MICAS Laboratory of the Katholieke Universiteit Leuven, where he worked in the field of mixed-signal design, modeling and design automation. In 2002, he was appointed as a Postdoctoral Research Assistant in the same research group. Since 2003, he has been with the Nomadic Embedded Systems division of the Interuniversitary Microelectronics Center (IMEC/NES), Belgium, where he has been working on signal integrity in mixed-signal systems and low-power scalable radios. He is currently coordinating the research on energy efficient data converters. He has been the author and co-author of over 75 papers in journals and conference proceedings.

"Advanced SiP Design for Signal and Power Integrity"

Joungho Kim
KIST

In order to meet intensively growing needs of extremely small form-factor semiconductor system solutions with sufficiently low cost for high-density and multi-function mobile platforms, 3D SiP has become the most promising design approach. However, heavily populated integration of multiples chips in three dimensional stacking structures on a multi-layer substrate in the SiP, inevitably yields considerable problems of signal integrity and power integrity, while clock speeds of the digital chips are steadily increasing and noise sensitive analog and RF circuits are contained in a same package. These problems can be even serious in 3D SiP based on vertical TSV type interconnections.

In this tutorial, design and analysis approaches will be introduced with the considerations of the signal integrity and power integrity at the high speed and low noise 3D SiP's. These unique methods are based on simultaneous and hierarchical chip-package co-design and modeling approaches. They can be applied to the designs of high-speed I/O, clock delivery network, and Power Distribution Network (PDN) in the SiP. In particular, several investigations will be presented, in which we observe high-frequency electromagnetic couplings between the chips and the package structures through I/O channel's and PDN's in the SiP.

Tutorial Outline:

Chapter I: SiP Design for Signal Integrity
- I.1 Signal integrity issues in SiP design
- I.2 High frequency channel loss, and 3D TSV-based interconnections
- I.3 Hybrid equalization designs and measurements
- I.4 Chip-package Co-designs of 3D clock distribution networks

Chapter II: SiP Design for Power Integrity
- II.1 Power integrity issues in SiP design
- II.2 Chip-package interactions in SiP
- II.3 PDN in TSV-based 3D IC
- II.4 Embedded passives and novel PDN structures in SiP

Dr. Joungho Kim received B.S. and M.S. degrees in electrical engineering from Seoul National University, in 1984 and 1986, respectively, and Ph.D degree in electrical engineering from the University of Michigan, Ann Arbor, in 1993. In 1996, he had joined KAIST (Korea Advanced Institute of Science and Technology). He is currently a Professor at Electrical Engineering and Computer Science Department. Since joining KAIST, his research centers on modeling, design, and measurement methodologies of 3D hierarchical

semiconductor systems including 3D IC and 3D SiP. Especially, his major research topic is focused on chip-package co-design and simulation methodologies with considerations of signal integrity, power integrity, ground integrity, timing integrity, and radiated emission in high-performance and low noise 3D IC and 3D SiP.

He has authored and co-authored over 230 technical papers in modeling, design, and measurement of 3D IC, 3D SiP, and multi-layer PCB. Also, he has given more than 105 invited talks and tutorials at academia and related industries. He has received 2006 Outstanding Academic Achievement Award of KAIST and 2008 Best Research Award of KAIST. Dr. Joungho Kim is the symposium chair of IEEE EDAPS 2008 Symposium. Currently, he is an Associated Editor of the IEEE Transactions of Electromagnetic Compatibility.

"Modern Clock Distribution System"

Simon Tam
Intel Corporation, USA.

Contemporary nano-meter scale CMOS process technologies enable a digital design to integrate a large amount of high performance digital circuits in a single die. A clock distribution system that is low skew, simple & efficient to implement, robust against process & voltage but is power efficient is a pre-requisite to such high performance digital designs. Clock distribution systems for high performance microprocessors are excellent examples where a robust clock system design provides a significant performance advantage. Additionally, the emergence of multi-core processors and highly integrated system-on-chip digital design, multi-clock domain clock distribution systems will become the norm. Although these designs will continue to be synchronous, the multi-clock domain distributions will need to accommodate multiple frequencies and pseudo-asynchronous interfaces.

This tutorial will present the fundamental clocking requirements, contemporary clock distribution architectures for power & skew using implementation examples from high performance microprocessors. Clock distribution topologies that include asymmetric and balanced clock tree networks, spines and grid structures, hybrid tree-grids and hybrid spine-grid structures are described. Additionally, tunable clock architectures with static or dynamic de-skew and design-for-test clocking techniques are presented. Multi-clock domains clocking architectures with mixed synchronous and pseudo-asynchronous interfaces like GALS and future directions on clock distributions will be outlined.

Outline:

1. Overview of clocking trends.
2. Fundamentals clocking requirements.
3. Clock distribution topologies and implementation examples.
4. De-skew techniques for clock distribution.
5. Debug features for clocking
6. Multi-clock domains clock distribution architectures and future directions.
7. Summary

Biography:

Simon Tam received the BS, MS, & Ph.D. degrees in Electrical Engineering & Computer Sciences from the University of California at Berkeley. He is presently a Senior Principal Engineer at Intel Corporation's Enterprise Microprocessors Group, where he has been focused on the implementation of clocking circuits for the Xeon® MP Processors. Prior to microprocessor circuit designs, he was engaged with the development of neural network and non-volatile memory technologies. He has authored or co-authored in 38 technical publications and holds 28 US patents. He is a Senior Member of the IEEE and member of the Technical Program Committee for the 2007 and 2008 IEEE Symposium on VLSI Circuits.

"Economic and Design Choices for Nanoscale Electronic Systems"

Siva G. Narendra Ph.D.
Co-Founder & CTO - Tyfone, Inc.

As the semiconductor industry consolidates its transition into the nanoscale era, challenges are abound. The existence of challenges for scaling semiconductor device dimensions is well known to the industry, and the solutions have primarily revolved around evolutionary intelligent engineering.

However, in the next two decades almost all of the dimensions of a nanoscale switch will approach atomic distances, should the pace of Moore's law continue. Therefore, the nature of solutions cannot just depend on evolutionary engineering, but will require fundamental breakthroughs in the sciences of materials and manufacturing. Depending on the manufacturable solutions that will emerge the overlaying design and architecture choices may have to be revolutionary.

Black box and deterministic design approach that has worked well in complex integrated systems thus far, with several layers of abstraction may need to be broken at least temporarily, to identify and implement the most suitable solution. The talk will describe technology and market trends; the challenges related to leakage, variation, yield, and cost; the source of these challenges; then discuss potential solutions for tackling them through evolutionary intelligent engineering methods and motivate a few nascent revolutionary concepts. Economic choices and technology design choices will be defined and presented. Technology choices including Pseudo Stochastic Design, Enhanced Stochastic Design, and True Stochastic Design will be discussed in detail.