A-SSCC 2011 SDC Candidates List

No.	Paper No.	1st Author	Affiliation	Country	Paper Title	Authors
SDC-1	P_07_1013	Mr. Kazutoshi Tomita	Keio University	Japan	1W 3.3V-to-16.3V Boosting Wireless Power Transfer Circuits with Vector Summing Power Controller	Kazutoshi Tomita, Ryota Shinoda, Tadahiro Kuroda, and Hiroki Ishikuro
SDC-2	P_07_1002	Mr. Joonsung Bae	KAIST	Republic of Korea	A Low Energy Crystal-Less Double-FSK Transceiver for Wireless Body-Area-Network	Joonsung Bae, Kiseok Song, Hyungwoo Lee, Hyunwoo Cho, and Hoi-Jun Yoo
SDC-3	P_06_1012	Ms. Deyun Cai	Fudan Univ.	China (P.R.C)	A 2.1-GHz PLL with −80dBc/−74dBc Reference Spur Based on Aperture-Phase Detector and Phase-to-Analog Converter	Deyun Cai, Haipeng Fu, Junyan Ren, Wei Li, Ning Li, Hao Yu, and Kiat Seng Yeo
SDC-4	P_04_1014	Mr. Chia-Ming Chang	National Taiwan University	Taiwan	A 172.6mW 43.8GFLOPS Energy-Efficient Scalable Eight-core 3D Graphics Processor for Mobile Multimedia Applications	Chia-Ming Chang, Yu-Jung Chen, Yen-Chang Lu, Chun-Yi Lin, Liang-Gee Chen, and Shao-Yi Chien
SDC-5	P_03_1030	Mr. Norihiro Kamae	Kyoto Univ.	Japan	An Area Effective Forward/Reverse Body Bias Generator for Within-Die Variability Compensation	Norihiro Kamae, Akira Tsuchiya, and Hidetoshi Onodera
SDC-6	P_05_1016	Mr. Hiroki Asada	Tokyo Institute of Technology	Japan	A 60 GHz 16 Gb/s 16QAM Low-Power Direct-Conversion Transceiver Using Capacitive Cross-Coupling Neutralization in 65 nm CMOS	Hiroki Asada, Keigo Bunsen, Kota Matsushita, Rui Murakami, Qinghong Bu, Ahmed Musa, Takahiro Sato, Tatsuya Yamaguchi, Ryo Minami, Toshihiko Ito, Kenichi Okada, and Akira Matsuzawa
SDC-7	P_02_1011	Ms. Yan Zhu	University of macau	Macao	A 35 fJ 10b 160 MS/s Pipelined-SAR ADC with Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation	Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, Rui Martins, and Franco Maloberti