Room A (Ramada Ballroom 1)

Session Title	**[Industry 1] System-on-Chip Innovations**
Session Chairs	Stefan Rusu (Intel Corporation, United States) Koji Kai (Panasonic Corp., Japan)
Date	November 15, 2011 (Tuesday)
Time	10:50~12:20

Industry 1-1	**10:50 - 11:20**	**An 18ms-Latency Wireless High Quality Codec SoC for Full HD Streaming** Pilsoon Choi, Yongseok Yi, Kilsik Ha, Yun-Gu Lee, Chil-Youl Yang, Seyoung Shin, Byung-Ho Ahn, Sung-Chul Park, Hyun-Tae Gil, Scott Lee, Joongsuk Park, and Jaemoon Jo
Industry 1-2	**11:20 - 11:50**	**The Second Generation Intel® Core™: a Highly Integrated High Performance Multi IA-Core and Processor Graphics Chip** Marcelo Yuffe, Omer Vikinski, Ziv Shmuely, Ernest Knoll, and Tsvika Kurts
Industry 1-3	**11:50 - 12:20**	**A Dynamic SIMD/MIMD Mode Switching Processor for Embedded Real-time Image Recognition Systems** shohei nomoto, shorin kyo, and shinichiro okazaki

Room B (Ramada Ballroom 2)

Session Title	**[Industry 2] Power and Signaling Building Blocks**
Session Chairs	Ron Ho (Oracle, Taiwan) Toru Shimizu (Renesas Electronics Corp., Japan)
Date	November 15, 2011 (Tuesday)
Time	10:50~12:20

Industry 2-1	**10:50 - 11:20**	**0.8-V Start-up 92% Efficiency On-Chip Boost DC-DC Converters for Battery Operation Micro-Computers**	Yasunobu Nakase, Shinichi Hirose, Toru Goda, Kehui Hu, Hiroshi Onoda, Yasuhiro Ido, Hiroyuki Kono, Wei Kong, Wei Zhang, Tsukasa Oishi, Shintaro Mori, and Toru Shimizu
Industry 2-2	**11:20 - 11:50**	**On Overcoming the Limitations of Single-Ended Signaling for Graphics Memory Interfaces**	Amir Amirkhany, Wendem Beyene, Chris Madden, Aliazam Abbasfar, Dave Secker, Dan Oh, Mohammad Hekmat, Ralf Schmitt, and Chuck Yuan
Industry 2-3	**11:50 - 12:20**	**Digitally-assisted analog circuits for a 10 Gbps, 395 fJ/b optical receiver in 40 nm CMOS**	Philip Amberg, Frankie Liu, Michael Dayringer, Jon Lexau, Dinesh Patil, Jon Gainsley, Hesam Fathi Moghadam, Elad Alon, Xuezhe Zheng, John Cunningham, Ashok Krishnamoorthy, and Ron Ho

Room A (Ramada Ballroom 1)

Session Title	**[Session 1] Power Management**
Session Chairs	Yasuhiro Sugimoto (Chuo University, Japan) Jeongjin Roh (Hanyang University, Korea)
Date	November 15, 2011 (Tuesday)
Time	13:30~15:35

1-1	**13:30 - 13:55**	**A 80-mV Input, 56 Times Faster Startup Dual-Mode Boost Converter with Charge-Pumped Pluse Generator for Energy Harvesting** Po-Hung Chen, Koichi Ishida, Xin Zhang, Yasuyuki Okuma, Yoshikatsu Ryu, Makoto Takamiya, and Takayasu Sakurai
1-2	**13:55 - 14:20**	**A 1.39-V Input Fast-Transient-Response Digital LDO Composed of Low-Voltage MOS Transistors in 40-nm CMOS Process** Masafumi Onouchi, Kazuo Otsuga, Yasuto Igarashi, Toyohito Ikeya, Sadayuki Morita, Koichiro Ishibashi, and Kazumasa Yanagisawa
1-3	**14:20 - 14:45**	**A High Stability DC-DC Boost Converter with Ripple Current Control and Capacitor-Free LDOs for AMOLED Display** Se-Won Wang, Young-Jin Woo, Sung-Ho Bae, Tae-Hwang Kong, Gyu-ha Cho, and Gyu-Hyeong Cho
1-4	**14:45 - 15:10**	**An Asynchronous Digitally-Controlled Switching Converter with Adaptive Resolution and Dynamic Power Saving to Achieve Higher Than 93.5% Efficiency between 5mA and 250mA Load** Po-Hsiang Lan, Tsung-Ju Yang, and Po-Chiun Huang
1-5	**15:10 - 15:22**	**A MOS Current-Mode Boost DC-DC Converter with the Duty-Ratio-Independent Frequency Characteristics** Yuya Hirano and Yasuhiro Sugimoto
1-6	**15:22 - 15:34**	**A Fast-Transient Quasi-V2 Switching Buck Regulator Using**

AOT Control

Huang Chun-Sheng, Wang Jia-Hui, Wang Chen-Yu, and Tsai Chien-Hung

Room B (Ramada Ballroom 2)

Session Title	**[Session 2] SAR and Binary-Search ADCs**
Session Chairs	Soon-Jyh Chang (National Cheng-Kung University, Taiwan) Yuichi Okuda (Renesas Electronics Corp., Japan)
Date	November 15, 2011 (Tuesday)
Time	13:30~15:35

2-1	**13:30 - 13:55**	**A 7-Bit 1.5-GS/s Time-Interleaved SAR ADC with Dynamic Track-and-Hold Amplifier** Masanori Furuta, Ippei Akita, Junya Matsuno, and Tetsuro Itakura
2-2	**13:55 - 14:20**	**A 35f J /conv-step 10b 160 MS/s Pipelined-SAR ADC with Self-Embedded Offset Cancellation** Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, Rui Martins, and Franco Maloberti
2-3	**14:20 - 14:45**	**A 10b Ternary SAR ADC with Decision Time Quantization Based Redundancy** Jon Guerber, Manideep Gande, Hariprasath Venkatram, Allen Waters, and Un-Ku Moon
2-4	**14:45 - 15:10**	**A 0.9-V 11-bit 25-MS/s Binary-Search SAR ADC in 90-nm CMOS** Ying-Zu Lin, Soon-Jyh Chang, Ya-Ting Shyu, Guan-Ying Huang, and Chun-Cheng Liu
2-5	**15:10 - 15:22**	**A 4.8-bit ENOB 5-bit 500MS/s Binary-Search ADC with Minimized Number of Comparators** Si-Seng Wong, U-Fat Chio, He-Gong Wei, Chi-Hang Chan, Hou-Lon Choi, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins
2-6	**15:22 - 15:34**	**Digital-Domain Calibration of Split-Capacitor DAC with no Extra Calibration DAC for a Differential-Type SAR ADC** Ji-Yong Um, Jae-Hwan Kim, Jae-Yoon Sim, and Hong-June Park

Room C (Ramada Ballroom 3)

Session Title	**[Session 3] Dividers, VCO & PLL**
Session Chairs	Chun Huat Heng (National University of Singapore, Singapore) Julien Ryckaert (IMEC / SSET, Belgium)
Date	November 15, 2011 (Tuesday)
Time	13:30~15:35

3-1	**13:30 - 13:55**	**A Low Power W-Band PLL with 17-mW in 65-nm CMOS Technology** Tao-Yao Chang, Chao-Shiun Wang, and Chorng-Kuang Wang
3-2	**13:55 - 14:20**	**A 20GHz ILFD with Locking Range of 31% for Divide-by-4 and 15% for Divide-by-8 Using Progressive Mixing** Ahmed Musa, Kenichi Okada, and Akira Matsuzawa
3-3	**14:20 - 14:45**	**An 85-GHz Injection-Locked Frequency Divider with Current-Reuse Pre-Amplifier Technique** Shu-Wei Chu and Chorng-Kuang Wang
3-4	**14:45 - 15:10**	**3.6mW D-band Divide-by-3 Injection-Locked Frequency Dividers in 65nm CMOS** I-Ting Lee, Chiao-Hsing Wang, and Shen-Iuan Liu
3-5	**15:10 - 15:22**	**A 0.13-μm SiGe HBT D-Band Divide-by-6 Injection-Locked Frequency Divider** Lei Wang, Yongzhong Xiong, Sanming Hu, and Teckguan Lim
3-6	**15:22 - 15:34**	**A 1.22/6.7 ppm/ oC VCO with Frequency-Drifting Compensator in 60 nm CMOS** Lan-Chou Cho, Hsiang-Hui Chang, Augusto Marques, Albert Yang, CS Chiu, and GK Dehng

Room D (Ramada Ballroom 4)

Session Title	**[Session 4] Ambient Sensing & Security**
Session Chairs	Shawn Shuo-Hung Hsu (National Tsinghua University, Taiwan) Ilku Nam (Pusan National University, Korea)
Date	November 15, 2011 (Tuesday)
Time	13:30~15:35

4-1	**13:30 - 13:55**	**A 1.8V 11μW CMOS Smart Humidity Sensor for RFID Sensing Applications** Zhichao Tan, Roel Daamen, Aurélie Humbert, Kamran Souri, Youngcheol Chae, Youri Ponomarev, and Michiel Pertijs
4-2	**13:55 - 14:20**	**A 0.6V to 1.6V, 46uW Voltage and Temperature Independent 48 MHz Pulsed LC Oscillator for RFID Tags** Valentijn De Smedt, Georges Gielen, and Wim Dehaene
4-3	**14:20 - 14:45**	**A 190mV supply, 10MHz, 90nm CMOS, Pipelined Sub-Threshold Adder using Variation-Resilient Circuit Techniques** Nele Reynders and Wim Dehaene
4-4	**14:45 - 15:10**	**Design and Demonstration of Micro-Electro-Mechanical Relay Multipliers** Hossein Fariborzi, Fred Chen, Rhesa Nathanael, Jaeseok Jeon, Tsu-Jae King Liu, and Vladimir Stojanovic
4-5	**15:10 - 15:35**	**Piezoresitive 6-MNA Coated Microcantilevers with Signal Conditioning Circuits for Electronic Nose** Neena Gilda, Sheetal Patil, Seena V, Sanjay Joshi, Viral Thaker, Sanket Thakur, Anvesha A, M.Shojaei Baghini, D.K. Sharma, and V.Ramgopal Rao

Room A (Ramada Ballroom 1)

Session Title	**[Session 5] Phase locked circuits & I/O links**
Session Chairs	Jri Lee (National Taiwan University, Taiwan)
	Hiroyuki Okada (Renesas Electronics Corporation, Japan)
Date	November 16, 2011 (Wednesday)
Time	10:25~12:30

5-1	**10:25 - 10:50**	**Extending HyperTransport™ Technology to 8.0 Gb/s in 32-nm SOI-CMOS Processors** Bruce A. Doyle, Alvin S. Loke, Sanjeev K. Maheshwari, Charles L. Wang, Dennis M. Fischette, Jeffrey G. Cooper, Sanjeev K. Aggarwal, TinTin Wee, Chad O. Lackey, Harishkumar S. Kedarnath, Michael M. Oshima, Gerry R. Talbot, and Emerson S. Fang
5-2	**10:50 - 11:15**	**A Leakage-Current-Recycling Phase-Locked Loop in 65nm CMOS Technology** I-Ting Lee, Yun-Ta Tsai, and Shen-Iuan Liu
5-3	**11:15 - 11:27**	**A 2.1-GHz PLL with −80dBc/−74dBc Reference Spur Based on Aperture-Phase Detector and Phase-to-Analog Converter** Deyun Cai, Haipeng Fu, Junyan Ren, Wei Li, Ning Li, and Hao Yu
5-4	**11:27 - 11:39**	**A 0.6V Noise Rejectable All-Digital CDR with Free Running TDC for a Pulse-Based Inductive-Coupling Interface** Won-Joo Yun, Hiroki Ishikuro, and Tadahiro Kuroda
5-5	**11:39 - 12:04**	**Injection-Locked Clock Receiver for Monolithic Optical Link in 45nm SOI** Jonathan Leu and Vladimir Stojanovic
5-6	**12:04 - 12:29**	**A 900 Mbps Single-Channel Capacitive I/O Link for Wireless Wafer-Level Testing of Integrated Circuits** Dae Young Lee, David Wentzloff, and John Hayes

Room B (Ramada Ballroom 2)

Session Title	**[Session 6] Memory**
Session Chairs	Sungdae Choi (Hynix Semiconductor Inc., Korea) Atsushi Kawasumi (Toshiba Corporation, Japan)
Date	November 16, 2011 (Wednesday)
Time	10:25~12:30

6-1	**10:25 - 10:50**	**A Low-Power Small-Area Open Loop Digital DLL for 2.2Gb/s/pin 2Gb DDR3 SDRAM** Jong-Chern Lee, Sin-Hyun Jin, Dae-Suk Kim, Young-Jun Ku, Chul Kim, Byung-Kwon Park, Hong-Gyeom Kim, Seong-Jun Ahn, Jae-Jin Lee, and Sung-Joo Hong
6-2	**10:50 - 11:15**	**A Trimless, 0.5V-1.0V Wide Voltage Operation, High Desity SRAM Macro Utilizing Dynamic Cell Stability Monitor and Multiple Memory Cell Access** Keiichi Kushida, Osamu Hirabayashi, Fumihiko Tachibana, Hiroyuki Hara, Atsushi Kawasumi, Azuma Suzuki, Yasuhisa Takeyama, Yuki Fujimura, Yusuke Niki, Miyako Shizuno, Shinichi Sasaki, and Tomoaki Yabe
6-3	**11:15 - 11:40**	**Energy Efficiency Degradation Caused by Random Variation in Low-Voltage SRAM and 26% Improvement by Bitline Amplitude Limiting (BAL) Scheme** Atsushi Kawasumi, Toshikazu Suzuki, Shinichi Moriwaki, and Shinji Miyano
6-4	**11:40 - 12:05**	**High-Voltage Wordline Generator for Low-Power Program Operation in NAND Flash Memories** Sam-Kyu Won, Yujong Noh, Hyunchul Cho, Jeil Ryu, Sungwook Choi, Sungdae Choi, Duckju Kim, Junseop Chung, Bongseok Han, and Eui-Young Chung
6-5	**12:05 - 12:30**	**Low Power Cross Point Memory Architecture** Chang Siau, Bruce Bateman, and Christophe Chevallier

Room C (Ramada Ballroom 3)

Session Title	**[Session 7] Circuits for Bio Sciences**
Session Chairs	Seungjun Lee (Ewha Womans University, Korea) Yusuke Kanno (Hitachi, Ltd., Japan)
Date	November 16, 2011 (Wednesday)
Time	10:25~12:30

7-1	**10:25 - 10:50**	**1W 3.3V-to-16.3V Boosting Wireless Power Transfer Circuits with Vector Summing Power Controller** Kazutoshi Tomita, Ryota Shinoda, Tadahiro Kuroda, and Hiroki Ishikuro
7-2	**10:50 - 11:15**	**A Low Energy Crystal-Less Double-FSK Transceiver for Wireless Body-Area-Network** Joonsung Bae, Kiseok Song, Hyungwoo Lee, Hyunwoo Cho, and Hoi-Jun Yoo
7-3	**11:15 - 11:40**	**An Omnidirectional Wireless Power Receiving IC with 93.6% Efficiency CMOS Rectifier and Skipping Booster for Implantable Bio-Microsystems** Tianjia Sun, Xiang Xie, Guolin Li, Yingke Gu, Xiaomeng Li, and Zhihua Wang
7-4	**11:40 - 12:05**	**A 0.67mW 14.55Mbps OFDM-Based Sensor Node Transmitter for Body Channel Communications** Tsan-Wen Chen, Ping-Yuan Tsai, Jui-Yuan Yu, and Chen-Yi Lee
7-5	**12:05 - 12:17**	**A 0.8V 64x64 CMOS Imager with Integated Sense-and-Stimulus Pixel for Artificial Retina Applications** Chih-Lin Lee and Chih-Cheng Hsieh
7-6	**12:17 - 12:29**	**A Programmable Muscle Stimulator Based on Dual-Slope Charge Balance** Jason Tan, Xu Liu, Keng Hoong Wee, Shih-Cheng Yen, and Yong Ping Xu

Room D (Ramada Ballroom 4)

Session Title	**[Session 8] Circuit Techniques for Robustness and Performance Enhancement**
Session Chairs	Utpal Desai (Intel Technology India Pvt. Ltd, India) Makoto Ikeda (University of Tokyo, Japan)
Date	November 16, 2011 (Wednesday)
Time	10:25~12:30

8-1	**10:25 - 10:50**	**An On-Chip Timing Jitter Measurement Circuit Using a Self-Referenced Clock and a Cascaded Time Difference Amplifier with Duty-Cycle Compensation** Kiichi Niitsu, Masato Sakurai, Naohiro Harigai, Takahiro J. Yamaguchi, and Haruo Kobayashi
8-2	**10:50 - 11:15**	**Rotary Coding for Power Reduction and S/N Improvement in Inductive-Coupling Data Communication** Andrzej Radecki, Noriyuki Miura, Hiroki Ishikuro, and Tadahiro Kuroda
8-3	**11:15 - 11:40**	**Correlations between Well Potential and SEUs Measured by Well-Potential Perturbation Detectors in 65nm** Jun Furuta, Ryosuke Yamamoto, Kazutoshi Kobayashi, and Hidetoshi Onodera
8-4	**11:40 - 12:05**	**A 1pJ/cycle Processing Engine in LDPC Application with Charge Recovery Logic** Yimeng Zhang, Mengshu Huang, Nan Wang, Satoshi Goto, and Tsutomu Yoshihara
8-5	**12:05 - 12:30**	**An Area Effective Forward/Reverse Body Bias Generator for Within-Die Variability Compensation** Norihiro Kamae, Akira Tsuchiya, and Hidetoshi Onodera

Room A (Ramada Ballroom 1)

Session Title	**[Session 9] Analog Techniques**
Session Chairs	Seung-Tak Ryu (KAIST, Korea)
	Tetsuya Hirose (Kobe University, Japan)
Date	November 16, 2011 (Wednesday)
Time	13:30~15:35

9-1	**13:30 - 13:55**	**A 106dB PSRR Direct Battery Connected Reconfigurable Class-AB/D Speaker Amplifier for Hands-free/Receiver 2-in-1 Loudspeaker** Kuo-Hsin Chen and Yen-Shun Shyu
9-2	**13:55 - 14:20**	**A CMOS Broadband Precise Programmable Gain Amplifier with Bandwidth Extension Technique** Nan Lin, Fei Fang, Zhi-Liang Hong, and Hao Fang
9-3	**14:20 - 14:45**	**An Efficient and Stable Power Management Circuit with High Output Energy for Wireless Powering Capsule Endoscopy** Liang Feng, Yu Mao, and Yuhua Cheng
9-4	**14:45 - 15:10**	**A Reconfigurable Low-Noise Dynamic Comparator with Offset Calibration in 90nm CMOS** Chi-Hang Chan, Zhu Yan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, and Rui Martins
9-5	**15:10 - 15:22**	**A 18.9-nA Standby Current Comparator with Adaptive Bias Current Generator** Kosuke Isono, Tetsuya Hirose, Keishi Tsubaki, Nobutaka Kuroki, and Masahiro Numa
9-6	**15:22 - 15:34**	**A 21-bit Read-Out IC Employing Dynamic Element Matching with 0.037% Gain Error** Rong Wu, Johan Huijsing, and Kofi Makinwa

Room B (Ramada Ballroom 2)

Session Title	**[Session 10] Sigma Delta Converters**
Session Chairs	Yong Ping Xu (National University of Singapore, Singapore) Hung Sung Li (Mediatek Inc., Taiwan)
Date	November 16, 2011 (Wednesday)
Time	13:30~15:35

10-1	**13:30 - 13:55**	**A Continuous-Time ΣΔ Modulator with a Gm-C Input Stage, 120-dB CMRR and -87 dB THD** Navid Sarhangnejad, Rong Wu, Youngcheol Chae, and Kofi Makinwa
10-2	**13:55 - 14:20**	**A 40MHz 12bit 84.2dB-SFDR Continuous-Time Delta-Sigma Modulator in 90nm CMOS** Xinpeng Xing, Maarten De Bock, Pieter Rombouts, and Georges Gielen
10-3	**14:20 - 14:45**	**A 0.06-mm2 Double-Sampling Single-OTA 2nd-order ΔΣ Modulator in 0.18-μm CMOS Technology** Kei-Tee Tiew and Minkyu Je
10-4	**14:45 - 15:10**	**A 102dB Dynamic Range Audio Sigma-Delta Modulator in 40nm CMOS** Tien-Yu Lo
10-5	**15:10 - 15:22**	**A 75.1dB SNDR, 80.2dB DR, 4th-order Feed-forward Continuous-Time Sigma-Delta Modulator with Hybrid Integrator for Silicon TV-tuner Application** Chen-Yen Ho, Zwei-Mei Lee, Mu-Chen Huang, and Sheng-Jui Huang
10-6	**15:22 - 15:34**	**A 4MHz BW 69dB SNDR Continuous-Time Delta-Sigma Modulator with Reduced Sensitivity to Clock Jitter** Yu-Chang Chang, Wei-Hao Chiu, Chen-Chien Lin, and Tsung-Hsien Lin

Room C (Ramada Ballroom 3)

Session Title	**[Session 11] RF Transmitter and Modulator**
Session Chairs	Tae Wook Kim (Yonsei University, Korea)
	Shuya Kishimoto (NEC Corporation, Japan)
Date	November 16, 2011 (Wednesday)
Time	13:30~15:35

11-1	**13:30 - 13:55**	**A 434GHz SiGe BiCMOS Transmitter with an On-Chip SIW Slot Antenna** Sanming Hu, Lei Wang, Yong Zhong Xiong, Bo Zhang, and Teck Guan Lim
11-2	**13:55 - 14:20**	**A 12-Element 60GHz CMOS Phased Array Transmitter on LTCC Package with Integrated Antennas** Ajay Balankutty, Stefano Pellerano, Telesphor Kamgaing, Kranti Tantwai, and Yorgos Palaskas
11-3	**14:20 - 14:45**	**A 2-GHz Digital I/Q Modulator in 65nm CMOS** Seyed Morteza Alavi, Akshay Visweswaran, Robert Bogdan Staszewski, Leo C.N de Vreede, John R Long, and Atef Akhnoukh
11-4	**14:45 - 15:10**	**A 15-mW 2.4-GHz IEEE 802.15.4 Transmitter with a FIR-Embedded Phase Modulator** Yao-Hong Liu, Hao-Hung Lo, and Tsung-Hsien Lin
11-5	**15:10 - 15:22**	**An Impedance Modulated Class-E Polar Amplifier in 90 nm CMOS** Mark Ingels, Vincenco Chironi, Bjorn Debaillie, Andrea Baschirotto, and Jan Craninckx
11-6	**15:22 - 15:34**	**A 3.4-mW 54.24-Mbps Burst-Mode Injection-Locked CMOS FSK Transmitter** Zhiming Chen, Kuang-Wei Cheng, Yuanjin Zheng, and Minkyu Je

Room D (Ramada Ballroom 4)

Session Title	**[Session 12] Digital Communication Systems**
Session Chairs	Robert Chen-Hao Chang (National Chung Hsing University, Taiwan) Hsie-Chia Chang (National Chia Tung University, Taiwan)
Date	November 16, 2011 (Wednesday)
Time	13:30~15:35

12-1	**13:30 - 13:55**	**A 7Gb/s SC-FDE/OFDM Baseband MMSE Equalizer for 60GHz Wireless Communications** Frank Hsiao, Derek Yang, Mike Pham, Adrian Tang, and Mau-Chung Frank Chang
12-2	**13:55 - 14:20**	**A 772 Mbit/s 8.81 bit/nJ 90 nm CMOS Soft-Input Soft-Output Sphere Decoder** Filippo Borlenghi, Ernst Martin Witte, Gerd Ascheid, Heinrich Meyr, and Andreas Burg
12-3	**14:20 - 14:45**	**A Micropower Biomedical Signal Processor for Mobile Healthcare Applications** Shu-Yu Hsu, Yao-Lin Chen, Po-Yao Chang, Jui-Yuan Yu, Ten-Fang Yang, Ray-Jade Chen, and Chen-Yi Lee
12-4	**14:45 - 14:57**	**A 22-Gb/s and over-33-mega-frame/s throughput bridge-function unit in a low-latency OLT LSI for the coexistence of 10G-EPON and GE-PON** Shoko Ohteru, Tomoaki Kawamura, Hiroki Suto, Masami Urano, Mamoru Nakanishi, and Tsugumichi Shibata
12-5	**14:57 - 15:09**	**A 684Mbps 57mW Joint QR Decomposition and MIMO Processor for 4×4 MIMO-OFDM Systems** Po-Lin Chiu, Lin-Zheng Huang, Li-Wei Chai, Chun-Fu Liao, and Yuan-Hao Huang
12-6	**15:09 - 15:21**	**A 6.6pJ/bit/iter Radix-16 Modified Log-MAP Decoder using Two-Stage ACS Architecture** Kai-Ting Shr, Yu-Cheng Chang, Chu-Yi Lin, and Yuan-Hao Huang

12-7 **15:21 - 15:33** **A 115mW 1Gbps QC-LDPC Decoder ASIC for WiMAX in 65nm CMOS**

Xiao Peng, Zhixiang Chen, Xiongxin Zhao, Dajiang Zhou, and Satoshi Goto

Room A (Ramada Ballroom 1)

Session Title	**[Session 13] Timing and Mixed Signal Techniques**
Session Chairs	Seng-Pan U (University of Macau, Macao) In-Chul Hwang (Kangwon National University, Korea)
Date	November 16, 2011 (Wednesday)
Time	15:55~18:00

13-1	**15:55 - 16:20**	**A low power Time-of-Arrival ranging front end based on a 8-channel 2.2mW, 53ps single-shot-precision Time-to-Digital Converter** Tom Redant, Frederic Stubbe, and Wim Dehaene
13-2	**16:20 - 16:45**	**A high-Gain Wide-Input-Range Time Amplifier with an Open-Loop Architecture and a Gain Equal to Current Bias Ratio** Hye-Jung Kwon, Jae-Seung Lee, Jae-Yoon Sim, and Hong June Park
13-3	**16:45 - 17:10**	**On-the-fly Dynamic Voltage Scaling (DVS) in 65nm Energy-Efficient Power Management with Frequency-Based Control (FBC) for SoC System** Yu-Huei Lee, Chao-Chang Chiu, Ke-Horng Chen, Ying-Hsi Lin, and Chen-Chih Huang
13-4	**17:10 - 17:35**	**A 0.2-0.6 V Ring Oscillator Design Using Bootstrap Technique** Yingchieh Ho, Yu-Sheng Yang, and Chauchin Su
13-5	**17:35 - 17:47**	**A 0.8V, Sub-mW, Varactor-Tuning Ring-Oscillator-Based Clock Generator in 32nm CMOS** Jenlung Liu, Sehyung Jeon, Tae-Kwang Jang, Dohyung Kim, Jihyun Kim, Jaejin Park, and Hojin Park
13-6	**17:47 - 17:59**	**Line Inversion-Based Mobile TFT-LCD Driver IC with Accurate Quadruple-Gamma-Curve Correction** Jae-Hyuck Woo, Jae-Goo Lee, In-Suk Kim, Young-Hyun Jun, Gyoo-Cheol Hwang, Myung-Hee Lee, and Bai-Sun Kong

Room B (Ramada Ballroom 2)

Session Title	**[Session 14] Nyquist Rate ADCs and Time-to-Digital Converters**
Session Chairs	Yong Moon (Soongsil University, Korea) Kwang-hyun Baek (Chung-Ang University, Korea)
Date	November 16, 2011 (Wednesday)
Time	15:55~18:00

14-1	**15:55 - 16:20**	**A 30% Beyond VDD Signal Swing 9-ENOB Pipelined ADC using a 1.2V 30dB Loop-Gain Opamp** B Robert Gregoire, Tawfiq Musah, Nima Maghari, Skyler Weaver, and Un-Ku Moon
14-2	**16:20 - 16:45**	**A 14-bit 200-MS/s Time-Interleaved ADC with Sample-Time Error Detection and Cancelation** Bei Yu, Chixiao Chen, Yu Zhu, Peng Zhang, Yiwen Zhang, Xiaoshi Zhu, Fan Ye, and Juyan Ren
14-3	**16:45 - 17:10**	**A Time-Domain Architecture and Design Method of High Speed A-to-D Converters with Standard Cells** MASAO TAKAYAMA, SHIRO DOSHO, NORIAKI TAKEDA, MASAYA MIYAHARA, and AKIRA MATSUZAWA
14-4	**17:10 - 17:35**	**A 90nm CMOS, 5.6ps, 0.23pJ/code Time-to-Digital Converter with Multipath Oscillator and Seamless Cycle Detection** Lai Chang-Ming, Shen Meng-Hung, Pan Geng-Yi, and Hunag Po-Chiun
14-5	**17:35 - 18:00**	**A 0.7mW 13b temperature-stable MASH ΔΣ TDC with delay-line assisted calibration** Ying Cao, Paul Leroux, Wouter De Cock, and Michiel Steyaert

Room C (Ramada Ballroom 3)

Session Title	**[Session 15] Techniques for transceiver integration**
Session Chairs	Baoyong Chi (Tsinghua University, China) Chien-Nan Kuo (National Chao Tung University, Taiwan)
Date	November 16, 2011 (Wednesday)
Time	15:55~18:00

15-1	**15:55 - 16:20**	**An Ultra-low-cost Bluetooth SOC in 0.11-um CMOS** Sam Chun-Geik Tan, Fei Song, Renliang Zheng, Jiqing Cui, guoqin Yao, litian Tang, yuejin Yang, dandan Guo, Alexander Tanzil, Junmin Cao, Ming Kong, Kiantiong Wong, Chee Lee Heng, Osama Shanaa, and GK Dehng
15-2	**16:20 - 16:45**	**An Energy-Efficient Super-Regenerative ASK Receiver with a DS-Based Pulse-Width Demodulator** Po-Yun Hsiao and Tsung-Hsien Lin
15-3	**16:45 - 17:10**	**A 60 GHz 16 Gb/s 16QAM Low-Power Direct-Conversion Transceiver Using Capacitive Cross-Coupling Neutralization in 65 nm CMOS** Hiroki Asada, Keigo Bunsen, Kota Matsushita, Rui Murakami, Qinghong Bu, Ahmed Musa, Takahiro Sato, Tatsuya Yamaguchi, Ryo Minami, Toshihiko Ito, Kenichi Okada, and Akira Matsuzawa
15-4	**17:10 - 17:35**	**A Low-Power Digital Front-end Direct-sampling Receiver for Flexible Radios** Rashmi Nanda, Henry Chen, and Dejan Markovic
15-5	**17:35 - 17:47**	**A High-Band IR-UWB Chipset for Real-Time Duty-Cycled Communication and Localization Systems** Xiaoyan Wang, Kathleen Philips, Cui Zhou, Benjamin Busze, Pieter Harpe, Hans Pflug, Alex Young, Jac Romme, Stefano D'Amico, Marcello De Matteis, Andrea Baschirotto, and Harmke De Groot
15-6	**17:47 - 17:59**	**An Active Guarding Technique for Substrate Noise**

suppression on LC-tank Oscillators

Hao-Ming Chao, Kuei-Ann Wen, and Michiel Steyaert

Room D (Ramada Ballroom 4)

Session Title	**[Session 16] Lowpower Circuits and Multimedia**
Session Chairs	Se-Joong Lee (Texas Instruments, U.S.A.) Sugako Otani (Renesas Electronics Corporation, Japan)
Date	November 16, 2011 (Wednesday)
Time	15:55~18:00

16-1	**15:55 - 16:20**	**An Asynchronous Mixed-mode Neuro-Fuzzy Controller for Energy Efficient Machine Intelligence SoC** Jinwook Oh, Gyeonghoon Kim, and Hoi-Jun Yoo
16-2	**16:20 - 16:45**	**System Performance and Energy Consumption Improvement Methodology by Delay Adjustable Synchronizer** Masanori Kurimoto, Yasuhiko Takahashi, Yuji Fujiwara, Mamoru Sakugawa, Soichi Kobayashi, and Hiroyuki Kondo
16-3	**16:45 - 17:10**	**A 92mW Real-Time Traffic Sign Recognition System with Robust Light and Dark Adaptation** Junyoung Park, Joonsoo Kwon, Jinwook Oh, Seungjin Lee, and Hoi-Jun Yoo
16-4	**17:10 - 17:35**	**Quad Full-HD Transform Engine for Dual-Standard Low-Power Video Coding** Rahul Rithe, Chih-Chi Cheng, and Anantha Chandrakasan
16-5	**17:35 - 18:00**	**A 172.6mW 43.8GFLOPS Energy-Efficient Scalable Eight-core 3D Graphics Processor for Mobile Multimedia Applications** Chia-Ming Chang, Yu-Jung Chen, Yen-Chang Lu, Chun-Yi Lin, Liang-Gee Chen, and Shao-Yi Chien