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<th>Session Title</th>
<th>[Session 2] SAR and Binary-Search ADCs</th>
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| Session Chairs | Soon-Jyh Chang (National Cheng-Kung University, Taiwan)  
Yuichi Okuda (Renesas Electronics Corp., Japan) |
| Date | November 15, 2011 (Tuesday) |
| Time | 13:30~15:35 |

2-1 13:30 - 13:55 A 7-Bit 1.5-GS/s Time-Interleaved SAR ADC with Dynamic Track-and-Hold Amplifier  
Masanori Furuta, Ippei Akita, Junya Matsuno, and Tetsuro Itakura

Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, Rui Martins, and Franco Maloberti

2-3 14:20 - 14:45 A 10b Ternary SAR ADC with Decision Time Quantization Based Redundancy  
Jon Guerber, Manideep Gande, Hariprasath Venkatram, Allen Waters, and Un-Ku Moon

2-4 14:45 - 15:10 A 0.9-V 11-bit 25-MS/s Binary-Search SAR ADC in 90-nm CMOS  
Ying-Zu Lin, Soon-Jyh Chang, Ya-Ting Shyu, Guan-Ying Huang, and Chun-Cheng Liu

2-5 15:10 - 15:22 A 4.8-bit ENOB 5-bit 500MS/s Binary-Search ADC with Minimized Number of Comparators  
Si-Seng Wong, U-Fat Chio, He-Gong Wei, Chi-Hang Chan, Hou-Lon Choi, Sai-Weng Sin, Seng-Pan U, and Rui P. Martins

2-6 15:22 - 15:34 Digital-Domain Calibration of Split-Capacitor DAC with no Extra Calibration DAC for a Differential-Type SAR ADC  
Ji-Yong Um, Jae-Hwan Kim, Jae-Yoon Sim, and Hong-June Park