Asymmetric Halo CMOSFET to Reduce Static Power Dissipation with Improved Performance

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***Abstract*— In this paper, the benefits of asymmetric halo (AH) MOSFETs over conventional symmetric halo (SH) MOSFETs to reduce static leakage in CMOS circuits have been presented. Device doping profiles have been optimized to obtain minimum leakage at iso on-current. Static leakage in AH devices is suppressed (61% in NMOS and 90% in PMOSFET) due to reduced band-to-band tunneling current in reverse biased drain-substrate junctions. At iso on-current, delay in AH ring-oscillator reduces by 11% because of reduced drain junction capacitance.**

I. Introduction

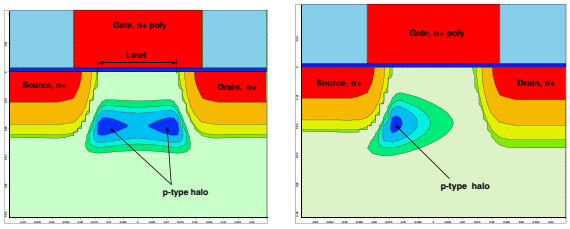
Scaling of MOS transistors has been extensively studied to improve circuit performance and packing density in the future VLSI circuits. However, the device scaling of MOSFETs is slowly approaching the physical limits of fabrication processes and devices. With each future technology generation, the dimensions of a MOSFET are drastically scaled down. Gate oxide cannot be scaled beyond a limit as gate direct tunneling leakage current increases exponentially with oxide thickness scaling. Also, voltage scaling is limited by the desired power supply-to-threshold voltage ratio (V_{dd}/V_t). V_t cannot be scaled too much to maintain adequate off-currents. Thus, with non-scaled gate oxide thickness and supply voltage, short-channel-effect (SCE) degrades in these devices. To suppress SCE, a laterally non-uniform (halo implants) doping profile has been suggested in [1]. Also, laterally asymmetric channel profile, i.e., different source and drain side peak halo doping concentrations (PHDC), was studied to improve hot carrier reliability [2] as well as performance [3].

In super-halo NMOSFETs, at high drain-to-substrate voltages, the n+ drain extension doping is reverse biased to the p-type halo implant. Since, supply voltage is not scaled as expected, there is high electric field at the n-p junction. This results in significant current flow due to the tunneling of electrons from the valence band of the p-region into the conduction band of the n-region. This reverse biased diode junction band to band tunneling (RBDJ BTBT) current density can be given by Kane's model [4]

$$J_{b-b} = \frac{\sqrt{2m^*}q^3\xi V}{4\pi^3\hbar^2 E_g^{1/2}} \; exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3q\xi\hbar}\right)$$

where E_g is the energy bandgap, V is the applied reverse voltage across the junction, ξ is the electric field and m^* is the effective mass of the electrons. RBDJ BTBT current is significant in the sub-50nm regime, where high doping concentration of halo implants is necessary to suppress SCE. It is shown that SCE are mainly controlled by the source-side halo doping [8]. In the most popular CMOS implementation of the circuits, drain-substrate junction is reverse biased and leaks RBDJ BTBT current. Therefore, drain side PHDC can be decreased to reduce RBDJ BTBT current. However, no extensive study has been done to explore the advantages of asymmetric halo devices (different source and drain side halos) in leakage reduction at iso-performance for the MOSFETs down to 25nm channel lengths.

This research is funded in part by Semiconductor Research Corporation under contract no. 1078.001.



(a) **(b)**

Fig. 1. Source, drain and halo doping contours in a 25-nm NMOSFET design with (a) Symmetric Halo, and (b) Asymmetric Halo.

In this work, static leakage and performance in asymmetric halo (AH) transistors have been compared, at device and circuit level, with conventional symmetric halo (SH) transistors. Doping contours and device geometry in symmetric and asymmetric halo MOSFETs are shown in Fig. 1. SH transistors have both source and drain side PHDCs of same concentration. AH transistors have different drain and source side PHDCs. Source side PHDC is normally higher than drain side PHDC to control SCE [8]. Two-dimensional device and mixed-mode circuit simulations have been performed in Taurus Device Simulator [5]. Taurus solves one-dimensional Schroedinger equation self-consistently with Poisson equation. It uses Kane's model [4] to compute the band-to-band tunneling carrier density. The carriers generated because of the band-to-band tunneling are included self-consistently.

II. Device Design

The basic device, on which modifications to doping profile are made, is 25nm channel length, well-tempered bulk-MOSFET from MIT [6]. Doping profiles have been optimized to obtain minimum leakage at iso on-current, by varying the concentration and position of PHDC. Moving up the peak halo on the source side, minimizes the penetration of lateral electric field from the drain to the source increasing the threshold voltage [7]. Also, moving down the position of peak halo degrades SCE and may result in punchthrough. Therefore the position of PHDC has been optimized first in symmetric halo devices to obtain maximum I_{on}/I_{off} ratio and then used as a fixed parameter. Devices do not show punchthrough.

A. Symmetric Halo (SH) MOSFETs

The doping profile of a symmetric halo device is optimized by varying PHDC on both the drain and the source sides equally. For an NMOS transistor in off-state ($V_{gs} = 0, V_{ds} = V_{dd}$), the total leakage current is supplied by the drain terminal. This includes (Fig. 2a) – gate direct tunneling current (I_{gdt}), subthreshold leakage current (I_{sub}) and RBDJ BTBT current (I_{btbt}) to substrate.

The leakage currents through the terminals of an NMOSFET, in its off-state, are shown in Fig. 2b against varying PHDC at drain and source sides. Halo concentration directly affects the channel doping concentration. Hence, threshold voltage increases with an increase in the PHDC resulting in reduced I_{sub}. Also, I_{btbt} increases because of increase in drain junction doping. Major component of the gate

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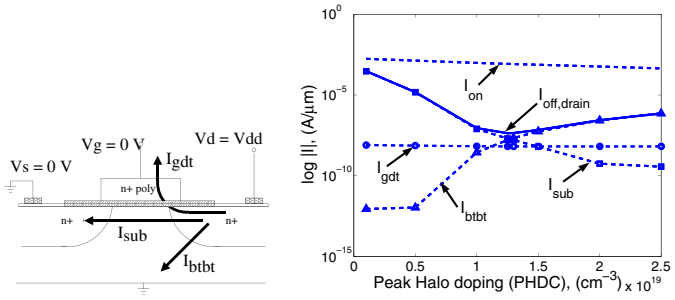

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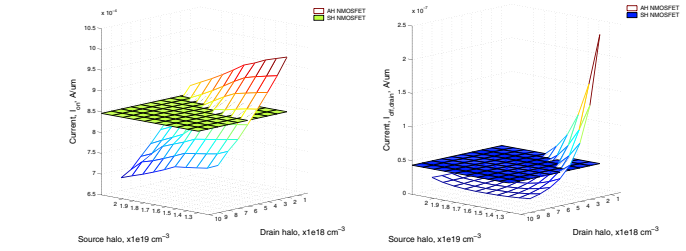
Fig. 2. (a) Major contributors to the off state leakage current in a SH NMOSFET, (b) for varying PHDCs.



(a) **(b)**

Fig. 3. Saturation and leakage currents in AH NMOSFET for different source and drain side halo doping concentrations. Horizontal planes refer to the current obtained in the designed SH NMOSFET. (a) on-current (I_{on}), (b) total leakage (I_{off}).

leakage in off-state is due to the gate to drain overlap. This component is independent of the channel doping, hence insensitive to the halo concentration. As expected, for the low values of halo concentration, I_{sub} is dominant and as the halo concentration increases, I_{btbt} dominates. Therefore in an NMOSFET, the total leakage is minimum at the S/D p-type PHDC of $1.3x10^{19}$ cm^{-3}. An NMOS transistor with this doping profile has been labeled as symmetric halo (SH) NMOS transistor.

Similar design and optimization approach has been adopted for a PMOS device. The optimum PHDC, to achieve minimum total off-state leakage, has been found to be $1.2x10^{19}$ cm^{-3}. Slight decrease in optimum PHDC in a PMOS, as compared to the SH NMOSFET, is because of higher I_{btbt} between the drain-substrate junctions in a PMOSFET. However, a doping profile complementary to the doping profile of the SH NMOSFET has been selected for the SH PMOSFET. This is not theoretically optimal and we do not get the minimum total leakage. However, it does not show too much deviation from the optimal doping profile.

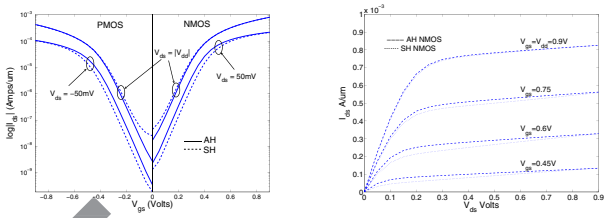
B. Asymmetric Halo (AH) MOSFETs

An NMOS transistor with the same geometry as SH NMOSFET is optimized by varying source and drain side PHDCs separately. It is optimized to obtain approximately the same on-current, as in SH NMOSFET, at minimum possible leakage. The aim is to minimize I_{btbt} by reducing the drain side PHDC. Also, source side PHDC needs to be increased to control SCE. Design space explored is – source side PHDC varying from $1.3x10^{19}cm^{-3}$ to $2x10^{19}cm^{-3}$ and drain side PHDC varying from $1x10^{18}cm^{-3}$ to $1x10^{19}cm^{-3}$. These values are chosen based on the range of terminal currents required. Fig. 3 shows I_{on} and I_{off} through the drain terminal for different source/drain PHDCs. It can be seen that the design window for the AH NMOSFET is strictly bounded by the required I_{on} and I_{off}. The optimal values of the source and drain side PHDCs to achieve minimum possible total

TABLE I

ELECTRICAL CHARACTERISTICS (LISTED AS {NMOS,PMOS})

Device parameters	SH Devices	AH Devices
Source side peak halo, cm^{-3}	$1.3x10^{19}$	$1.6x10^{19}$
Drain side peak halo, cm^{-3}	$1.3x10^{19}$	$6x10^{18}$
I_{on}, $\mu A/\mu m$	826.2,431.8	827.1,434.8
I_{drain}, $nA/\mu m$, off-state	44.5,27.8	17.2,3
I_{source}, $nA/\mu m$, off-state	16.1,3.2	10,1.7
$I_{substrate}$, $nA/\mu m$, off-state	21.9,24	0.36,0.4
I_{gate}, $nA/\mu m$, off-state	6.6,0.57	6.8,0.86
DIBL, mV/V	114,122	65,70
Sub. Swing, mV/dec	98,104	92,95



(a) **(b)**

Fig. 4. (a) I_{ds}-V_{gs} characteristics for AH and SH NMOS and PMOS transistors, (b) I_{ds}-V_{ds} characteristics for SH and AH NMOS devices.

leakage at the desired on-current are $1.6x10^{19}cm^{-3}$ and $6x10^{18}cm^{-3}$, respectively.

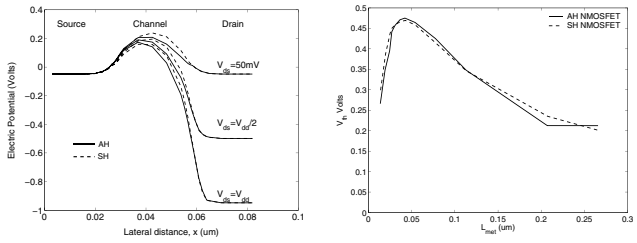
A doping profile complementary to the doping profile of the AH NMOSFET, has been found to be optimal in AH PMOSFET. This is because of reduced I_{btbt} in AH PMOS transistors.

C. Comparison of Device Characteristics

The electrical parameters for the SH and AH transistors are shown in Table I. Fig. 4a shows I_{ds}-V_{gs} characteristic of the designed SH and AH transistors. As can be seen, for the same I_{on}, there is a slight improvement in the subthreshold swing in AH transistor, which results in reduced I_{off}. Fig. 5a shows the conduction barrier in the channel near the Si/SiO_2 interface in designed SH and AH NMOSFETs. The barrier seen by the electrons, injected in the channel by the source, depends on the doping density at the source junction. As can be seen from the figure, high halo doping on the source side in the AH NMOSFET reduces Drain Induced Barrier Lowering (DIBL). However, drain side halo doping cannot be completely removed as it will affect the average channel doping and hence threshold voltage will be affected. Fig. 5b shows the saturation threshold voltage roll-off as a function of gate length. The threshold voltage roll-off of the SH and AH transistors is approximately same because of the approximately same subthreshold slope and iso on-current.

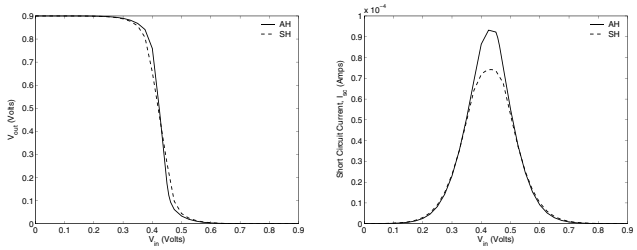
The I_{ds}-V_{ds} characteristic for the SH and AH NMOSFETs are shown in Fig. 4b. Saturation drain current, I_{dsat}, is high in AH NMOSFETs because of the lower vertical electric field at the drain end of the channel resulting in higher effective mobility.

It can be observed that AH MOSFETs have well defined source and drain terminals that has interesting implications for circuit implementation. For an AH NMOSFET, V_{ds} should never be negative and for an AH PMOSFET, V_{ds} should never be positive. Source and drain mismatch results in a bad device, i.e., if we use heavy halo doped side as drain terminal, then advantages on DIBL and I_{on}/I_{off} ratio will be lost. Therefore, AH MOSFETs can only be used in circuit styles where, at the design level, we are very well aware of the transistor's functionality. Because of these constraints, some logic styles such as pass-transistor logic are not feasible using AH MOSFETs. However, standard CMOS circuit style is very well-suited for AH transistors.



(a) **(b)**

Fig. 5. (a) Conduction band diagrams near the Si/SiO_2 interface in AH and SH NMOSFETs for different drain voltages (V_{ds}). In each case V_{gs} = 0V, (b) Saturation threshold voltage roll-off.



(a) **(b)**

Fig. 6. (a) Voltage Transfer Characteristics of a static CMOS inverter, (b) Short Circuit Current vs input voltage in static CMOS inverter.

III. Performance and Power

Performance and power consumption are analyzed for a 3-stage ring oscillator (RO) circuit. Each stage of the RO is a static CMOS inverter. The width ratio of PMOS to NMOS is $2\mu m : 1\mu m$ ($\simeq I_{on,NMOS}/I_{on,PMOS}$) to maximize the noise margins and obtain symmetrical characteristics. Voltage transfer characteristics and short-circuit currents in SH and AH CMOS inverters are shown in Fig. 6. The gain during switching is high in AH inverter because of reduced subthreshold swing and DIBL. This results in higher peak short-circuit current and improved noise-margins in AH inverter.

A. Performance Analysis

Gate input capacitance calculated by the small-signal analysis is 0.6fF. A constant lumped capacitance of 3.6fF (equal to the fanout of 2 inverters) is connected at the output of each stage. The stage delay in AH RO is 35.6ps compared to the stage delay of 39.8ps in SH RO. Delay reduces by 10.6% in AH RO compared to SH RO. This is attributed to the reduced drain junction capacitance in AH MOSFET because of reduced drain side PHDC.

B. Power Dissipation

1) Static Power: When the input of an inverter is logic '0', NMOS transistor is off and the leakage currents, going to the terminals at zero voltage, contribute to the static power dissipation. In PMOS, main leakage component is I_{gdt} and in NMOS all the three components of leakage current – I_{sub}, I_{btbt} and I_{gdt} – contribute to the total static leakage. For the input logic '1', NMOS leakage mainly includes I_{gdt} and in PMOS all the three components of the leakage current contribute to the total static leakage. The static power dissipation is given by

$$P_{static} = (I_{sub} + I_{btbt} + I_{gdt})V_{dd} = I_{leak}V_{dd}$$

Table II shows the leakage current components and total static power dissipation in SH and AH inverters. It can be seen that in AH inverter, I_{btbt} is greatly reduced, however, I_{gdt} in the ON transistor (NMOS for input '1' and PMOS for input '0') is dominant. Static power dissipation in AH inverter is approximately 76% of SH inverter for input '0' and 83% for input '1'. This results in average savings of 19% in AH inverter. At device level, the total static leakage in off-state in the AH NMOS transistor is 61% less than that in the SH NMOS transistor and total static leakage in the AH PMOS transistor is approximately 90% lower compared to the SH PMOS transistor.

2) Dynamic Energy: Dynamic energy consumption is due to the (1) charging/discharging of load capacitance, E_{C_L}, and (2) direct path currents from V_{dd} to ground, E_{dp}. The total dynamic energy is given by

$$E_{C_L} = V_{dd}\int_{t_1}^{t_1+T} i_{C_L}dt$$
$$E_{dp} = V_{dd}\int_{t_1}^{t_1+T} (i_{sub} + i_{btbt})dt$$
$$E_{dyn} = E_{C_L} + E_{dp}$$

where T=35.6ps for the AH RO circuit and T=39.8ps for the SH RO circuit; t_1 is an arbitrarily chosen time instant.

Dynamic energy consumption is computed in a single stage of the RO during falling and rising transitions. The results of dynamic energy calculations are shown in Table II. E_{dp} is comparatively higher in the AH RO because of higher peak short-circuit current during switching (Fig. 6). However, E_{C_L} is less in AH RO because of reduced drain junction capacitance. Hence, total dynamic energy consumption is approximately same in SH and AH ROs. Summing all the components of the power consumption, the total power consumption in a static CMOS inverter is expressed as

$$P_{total} = P_{static} + E_{dyn}f$$

where f is the clock frequency.

This implies that AH CMOSFETs are more effective in saving total power dissipation when the clock frequency is low and during standby (when static power is dominant).

IV. Static Power in CMOS Logic

We now consider 2-input static CMOS NAND logic gate. Since, reduced static power dissipation is the main advantage of AH circuits over SH circuits and dynamic energy consumption is almost same in both the devices, we will evaluate the static leakage currents in the pull down and pull up networks of the logic gates. Transistors are sized to obtain similar rise and fall propagation delays.

The study of static CMOS NAND gates is important because of the stacked NMOS transistors. Static power can be minimized in standby mode by forcing proper logic input combination [9]. The intermediate node voltage in the pull down network and DIBL of the transistors play an important role in determining the total leakage. The different components of leakage currents have been compared in SH and AH NAND gates for possible input logic combinations – '00', '10', '01' and '11'. The contribution of each input combination to the leakage current is discussed. Fig. 7 shows the major leakage components in a static CMOS 2-input NAND gate for different input logic combinations. Fig. 8 shows quantitavely the contribution of each input combination to the leakage.

Case I: Input '00': (Fig.7(a)) In this case, the drain and substrate junctions of the upper NMOS transistor are highly reverse biased and leak I_{btbt} in SH NAND gate. However, this component of leakage is aggressively suppressed in AH NAND gate. Intermediate node voltage is around 0V, hence, bottom transistor's substrate current is not significant. I_{gdt} is same in both the circuits and I_{sub} in AH NAND gate is higher than in SH NAND gate. This is because of reduced DIBL in AH devices which subdues the effects of transistor stacking [9].

Case II: Input '10' (Fig.7(b)) In this case, the source-substrate junction in the upper NMOSFET is reverse biased at the intermediate node voltage of $V_{dd} - V_t$. Because of the high source side PHDC in AH MOSFETs, I_{btbt} from the source to the substrate in the upper

TABLE II

STATIC POWER AND DYNAMIC ENERGY DISSIPATION IN AN INVERTER STAGE OF RO

	Static Power						Dynamic Energy		
	Input '0'			Input '1'					
	$I_{leak.NMOS}$	$I_{leak.PMOS}$	P_{static}	$I_{leak.PMOS}$	$I_{leak.NMOS}$	P_{static}	E_{C_L}	E_{dp}	E_{dyn}
SH	44.6nA	67.6nA	101nW	55.6nA	238.7nA	264.9nW	6.58fJ	6.37fJ	12.95fJ
AH	17.2nA	67.6nA	76.3nW	5.2nA	238.7nA	219.5nW	6.51fJ	6.43fJ	12.94fJ

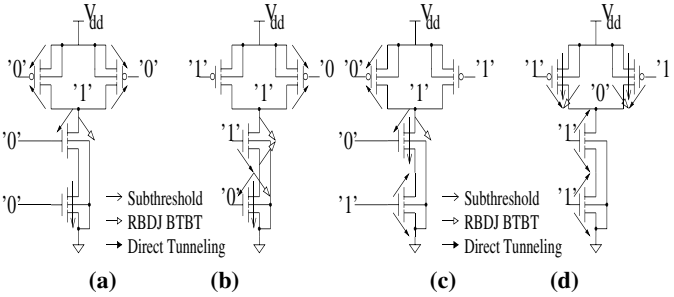


Fig. 7. Major leakage components in a SH NAND gate for different input combinations: (a) Case-I, input '00', (b) Case-II, input '10', (c) Case-III, input '01', and (d) Case-IV, input '11'.

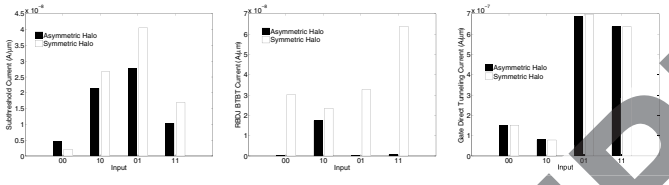


Fig. 8. Leakages in AH and SH NAND gates for different inputs: (a) I_{sub}, (b) I_{btbt}, and (c) I_{gdt}.

NMOSFET is comparatively high in AH NAND gate. This logic input combination is not able to utilize the leakage benefits in AH NAND gate because of the increased I_{btbt} in bottom transistor. However, total I_{btbt} is still less in AH NAND gate because of the reduced drain to substrate I_{btbt} in the upper NMOS transistor.

Case III: Input '01' (Fig.7(c)) In this case, the intermediate node voltage in the pull down network is around 0V. I_{btbt} flows in the upper NMOS transistor from the drain to the substrate. In this case, I_{gdt} dominates in the bottom transistor and nullifies the savings achieved due to the reduced I_{btbt} in AH devices.

Case IV: Input '11' (Fig.7(d)) In this case, the pull down network is on and only leakage component is gate direct tunneling current. However, pull up network is off and both the PMOS transistors leak I_{sub}, I_{btbt} and I_{gdt}.

V. IMPACT OF PROCESS VARIATIONS

With the scaling of technology, process imperfection is becoming a major concern in maintaining the reliability of the devices. We analyze the impact of simultaneous metallurgical gate length (L_{met}) and oxide thickness (T_{ox}) variations on the threshold voltage and on and off currents of the SH and AH transistors. Tolerances of 15% in channel length and 1Å in oxide thickness are used in the analysis.

Fig. 9 shows the worst case variations in I_{on} and I_{off} in NMOS and PMOS FETs. Reduction in I_{on} from its nominal value is maximum for +3σ variations in L_{met} and T_{ox}. Therefore delay is expected to be worst for +3σ variations in L_{met} and T_{ox}. Drop in I_{on} is 14% in AH NMOS and 20% in PMOS FETs of their corresponding nominal values. In SH NMOSFETs and PMOSFETs, on-current drops 30% from its nominal value. As expected, delay in a SH ring-oscillator increases 85% and delay in a AH ring-oscillator increases 50%. Off-current includes I_{sub}, I_{btbt} and I_{gdt}. I_{gdt} increases exponentially with

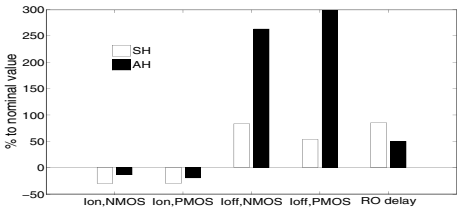


Fig. 9. Worst case variations in I_{on}, I_{off} and RO delay.

decrease in T_{ox} and I_{sub} increases exponentially with decrease in gate length. Therefore, off-current, increases significantly for -3σ variations in L_{met} and T_{ox}.

VI. CONCLUSION

In this paper asymmetric halo bulk-MOSFETs have been advocated over conventional symmetric halo MOSFETs for sub-50nm gate lengths. Devices have been optimized to achieve minimum leakage at iso on-current. AH MOSFETs have negligible band-to-band tunneling leakage in the reverse biased drain-substrate junctions and comparatively lower subthreshold leakage. Therefore, AH transistors dissipate comparatively less static power in the circuits. Dynamic energy is almost same in both the devices. However, circuits designed using AH transistors show improvement in the performance. This is because of reduced drain side halo doping concentration which reduces drain junction capacitance. AH devices come with some disadvantages as well. First, there is a need of one extra fabrication stage. This is because source and drain halos are to be doped using different masks. Second, for AH circuits, layout softwares need to be modified to identify source and drain terminals and connect them in a proper manner. Finally, logic styles, such as pass-transistor circuits are not possible with AH MOSFETs because of the constraint on well-defined source and drain terminals.

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