A-SSCC 2012

The 8th

IEEE Asian Solid-State Circuits Conference

Kobe, November 12-14, 2012

Advance Program

http://www.a-sscc2012.org

A-SSCC 2012 Program at Glance

Nov.12 (Mon.)				
Time	Room 401 4F	Room 402 4F	Reception Hall 3F	Lobby 4F
9:00 - 9:30 (30')				On-Site Registration (9:00-17:30)
9:30 - 10:50 (80')	Tutorial I "SoC Power Reduction and Management Techniques" Stefan Rusu (Intel)	Tutorial II "Designing CMOS Wireless LAN System-on-a-Chip" Srenik Mehta (Qualcomm Atheros)		
10:50 - 11:05 (15')	Break			
11:05 - 12:25 (80')	Tutorial I "SoC Power Reduction and Management Techniques" Stefan Rusu (Intel)	Tutorial II "Designing CMOS Wireless LAN System-on-a-Chip" Srenik Mehta (Qualcomm Atheros)		
12:25 - 13:25 (60')	Lunch			
13:25 - 14:45 (80')	Tutorial III "High Performance Non-Volatile Memory Design in Nano-Scale Era" Dr. Sungdae Choi (SK hynix Inc.)	Tutorial IV "Smart Sensor Design in Standard CMOS" Prof. Kofi Makinwa (Delft Univ. of Technology)		
14:45 - 15:00 (15')	Break			
15:00 - 16:20 (80')	Tutorial III "High Performance Non-Volatile Memory Design in Nano-Scale Era" Dr. Sungdae Choi (SK hynix Inc.)	Tutorial IV "Smart Sensor Design in Standard CMOS" Prof. Kofi Makinwa (Delft Univ. of Technology)		
16:20 - 17:30 (70')				
17:30 - 19:30 (120')	Welcome Reception (Reception Hall) Reception (Nov. 12) and Banquet (Nov. 13) are supported by industry supporters. We sincerely thank our industry supporters for A-SSCC 2012.		SDC Exibition (16:00-18:30)	
19:45 - 20:45 (60')	TCP Meeting (Room 401)			

Nov. 13 (Tue.)						
Time	International Conference Room Room 301 3F	Room 406	Room 401,Room 402 4F	Room 403	Reception Hall 3F	Lobby
8:30 - 9:00 (30')						On-Site Registration (8:30-17:30)
9:00 - 9:10 (10')	Opening Ceremony					
9:10 - 9:20 (10')	Welcome Speech					
9:20 - 10:05 (45')	Plenary Talk 1 "Expectations for the Semiconductor Techaologies in EVs and HVs" Mr. Shoichi Sasaki (Professor, Keio Univ.)					
10:05 - 10:50 (45')	Plenary Talk 2 "Semiconductor Memory Scaling and Beyond" Dr. Sungsoo Hong (SVP, SK hynix Inc., Korea)					
10:50 - 11:05 (15')	Break				SDC Exhibition	Supporter's Exhibition
11:05 - 12:45 (10')	Industry Program 1 Leading Edge SoCs and Memory		Industry Program 2 Energy Efficient Circuits for Emerging Applications			
12:45 - 13:45 (60')	Lunch					
13:45 - 15:50 (12')	Session 1 Analog Interfaces and Amplifiers	Session 2 Advanced Memory	Session 3 TX RX Architecture and Building Blocks	Session 4 Energy Efficient Circuits and Techniques		
15:50 - 16:05 (15')	Break				SDC Exhibition	
16:05 - 17:45 (10')	Panel Discussion 1 Disruptive design for emerging technology after 3D Devices/FinFET and beyond; How can we make it?		Panel Discussion 2 Challenge for Zero Stand-by Power Management - Road-map to the "Normally-Off Computing" -			
17:45 - 18:00 (15')						
18:00 - 18:30 (30')	Move to Cruiser					
19:00-21:20 (140')	Banquet (Kobe Cruise) We sincerely thank our industry supporters for A-SSCC 2012 Reception (Nov. 12) and Banquet (Nov. 13)					

Nov.14 (Wed.)						
Time	International Conference Room Room 301 3F	Room 401	Room 402 4F	Room 403	Reception Hall 3F	Lobby
8:30 - 9:00 (30')						On-Site Registration (8:30-12:00)
9:00 - 9:45 (45')	Plenary Talk 3 "Integrated Circuits and Systems toward Smart Ubiquitous Patient-Centered Medical Environment" Dr. Ming-Fong Chen (Superintendent, NTU)					
9:45 - 10:30 (45')	Plenary Talk 4 "Technology Challenges and Opportunities for Ubiquitous Computing" Dr. Shekhar Borkar (Intel Fellow, Intel Corp., U.S.A.)					
10:30 - 10:45 (15')	Break					
10:45 - 12:50 (12')	Session 5 High speed Transceivers and Building Block	Session 6 Nyquist-Rate ADCs	Session 7 Emerging Biomedical Circuits and Systems	Session 8 Low-Power Digital Communication & Multimedia SoCs	Supporter's Exhibition	
12:50 - 13:50 (60')	Lunch					
13:50 - 15:55 (12')	Session 9 Power Management ICs	Session 10 Oversampling ADCs	Session 11 Millimeter-Wave Circuits and Systems	Session 12 Clock Generation and Timing Circuits		
15:55 - 16:10 (15')	Break					
16:10 - 18:15 (125')	Session 13 SSD Memory and High Frequency Analog	Session 14 Ultra Low-Power Circuits for Emerging Communication System	Session 15 VCO & PLL	Session 16 Low-Power SoCs & Circuits		

Technical Program

Tutorials

November 12, 2012 (Monday)

Tutorial 1

Time: 9:30 - 12:25

Room: 401

SoC Power Reduction and Management Techniques

Stefan Rusu

Intel, USA

Abstract: CMOS process technology scaling has enabled higher feature integration in system-on-chip with multiple CPU and graphics cores and larger on-die caches. Reducing and managing power consumption is the most challenging task in today’s highly complex systems. In this tutorial, we will review power reduction and management techniques implemented in recent microprocessor and SoC designs, covering the entire spectrum from server to handheld applications. We will review flip-flop power optimization techniques, clock loading reduction, low-voltage operation, leakage reduction techniques, dynamic voltage and frequency scaling, and fine-grain power management techniques. Special attention will be devoted to adaptive circuit techniques that reduce the voltage and frequency design guard-bands. This tutorial includes recent innovations and practical examples from both industry and academic research

Biography: Stefan Rusu received the MSEE degree from the Polytechnic University in Bucharest, Romania. His industry experience includes 20 years with Intel Corp. and 6 years at Sun Microsystems. He is presently a Senior Principal Engineer in Intel's Microprocessor and Graphics Division leading the technology and special circuits design for the Xeon® Processors. Stefan has authored over 90 papers on VLSI circuit technology and holds 35 U.S. patents. He is an IEEE Fellow and a member of the Technical Program Committee for ISSCC, ESSCIRC and A-SSCC conferences. Stefan is an Associate Editor of the IEEE Journal of Solid-State Circuits and an elected member of the SSCS AdCom.

Tutorial 2

Time: 9:30 - 12:25

Room: 402

Designing CMOS Wireless LAN System-on-a-Chip

Srenik Mehta

Qualcomm Atheros, USA

Abstract: Wireless LAN SoCs are ubiquitous today in mobile, computing, and consumer electronics. The simultaneous push for low-cost and high-performance has necessitated the use of scaled CMOS technology with extensive use of digital calibration. This tutorial provides an overview of the challenges in designing CMOS wireless LAN System-on-a-Chip from the perspective of an analog/RF designer. An overview of transceiver building blocks, integration issues, and calibration techniques are described. Two system-on-a-chip examples are presented to contrast the techniques required for low-cost highly integrated 1x1 WLAN SoC versus a high-performance 3x3 WLAN SoC.

Biography: Srenik Mehta is a Sr Director of Engineering at Qualcomm Atheros, where he is engaged in the development of analog, mixed-signal and RF integrated circuits for wireless communication products. Srenik received the B.S. and M.S. degrees in electrical engineering from the University of California, Berkeley, in 1992 and 1997, respectively. From 1995 to 2000, he worked as a Senior Design Engineer at Level One Communications (now Intel Corporation), San Francisco, CA, where he designed CMOS RF and mixed-signal ICs for cordless telephones. Since February 2000, he has been with Atheros Communications (now Qualcomm Atheros), San Jose, California. He has been serving on the RFIC Symposium technical committee since 2005.

Tutorial 3

Time: 13:25 - 16:20

Room: 401

High Performance Non-Volatile Memory Design in Nano-Scale Era

Dr. Sungdae Choi, SK hynix

Abstract: Increase in the digital multimedia appliances such as mp3 player, digital camera brought huge demand for large capacity non-volatile memory (NVM) as a mobile storage device. And Solid-Sate Disk (SSD) is also getting into the spotlight. NAND Flash memory occupies the biggest portion among the non-volatile memory devices due to the small cell size and the maturity of the fabrication process, although it has the inherent disadvantage such as the slow write time and need of extra operations. Emerging NVM devices such as PCRAM and magnetic RAMs are expected as the next generation NVMs which succeeds the NAND Flash memory. This tutorial covers the problems and breakthrough of NAND Flash memory, introduction of expecting NVM devices and shows how they can work together to achieve the synergy effect. Multi-core processors demand larger on-die memories in order to maximize

Biography: Sungdae Choi received the B.S., M.S. and Ph.D. degrees from KAIST, Daejeon, Korea, in 2001, 2003 and 2006, respectively. His research field included application-specific-memory applications and body sensor network architecture. From 2006 to 2008, he joined Sakurai Lab. in the university of Tokyo, Japan, as a post-doctoral researcher and worked for the design for manufacturability project. From 2008 to 2009, he joined KAIST as a post-doctoral researcher and wrote the book titled Revised DRAM Design which will be published in 2012. In 2009, he joined SK hynix where he is currently working as a senior engineer at the Flash Development Division. Recently, he is also serving as a technical program committee member of ISSCC and ASSC.

Tutorial 4

Time: 13:25 - 16:20

Room: 402

Smart Sensor Design in Standard CMOS

Prof. Kofi Makinwa, Delft University of Technology

Abstract: Smart sensors are everywhere! They can be found in our homes, our cars and in nearly all mobile phones. However, processing weak sensor signals is quite challenging, especially when it must be done in standard CMOS, whose precision is limited by 1/f noise, component tolerances and mismatch. In this tutorial, a system approach to the design of smart sensors will be presented. The use of dynamic techniques, such as chopping, auto-zeroing, dynamic element matching and sigma-delta modulation, to trade speed for precision will be discussed. Examples will be given of state-of-the-art CMOS smart sensors for the measurement of temperature, humidity, magnetic field and even wind velocity.

Biography: Kofi A.A. Makinwa is a Professor at Delft University of Technology, where he leads a group that designs precision analog circuits, ΣΔ modulators, and smart sensors. This has resulted in 4 books, 17 patents and over 160 technical papers, many of which have received best paper awards: from the ISSCC, ESSCIRC, Transducers and JSSC among others. Dr. Makinwa has presented tutorials at several conferences and has served on the TPC of ISSCC and as an IEEE distinguished lecturer. He is currently on the TPC of ESSCIRC and the Advances in Analog Circuit Design (AACD) workshop, He is an IEEE fellow and an elected member of the IEEE SSCS AdCom.

Student Design Contest

November 12, 2012 (Monday)

Student Design Contest

Time: 16:00 - 18:30

Room: Reception Hall 3F

[SDC1] A 1.55mW Mixed-Signal Integrating Mixer for Direct Spectrum Estimation in 0.13um CMOS
Kevin Banovic, University of Toronto, Canada

[SDC2] A Built-in Self-Adjustment Scheme with Adaptive Body Bias Using P/N-Sensitive Digital Monitor Circuits
Islam A.K.M Mahfuzul, Kyoto University, Japan

[SDC3] Monitoring Effective Supply Voltage Within Power Rails of Integrated Circuits
Takeshi Okumoto, Kobe University, Japan

[SDC4] A 40nm CMOS Full Asynchronous Nano-Watt SAR ADC with 98% Leakage Power Reduction by Boosted Self Power Gating
Ryota Sekimoto, Keio University, Japan

[SDC5] Ultrasonic Imaging Front-End Design for CMUT: a 3-Level 30Vpp Pulse-Shaping Pulser with Improved Efficiency and a Noise-Optimized Receiver
Kailiang Chen, MIT, U.S.A

[SDC6] A 40 nm 535 Mbps Multiple Code-Rate Turbo Decoder Chip Using Reciprocal Dual Trellis
Chen Yang Lin, National Chiao Tung University, Taiwan

[SDC7] A Package Bondwire Based 80% Efficiency 80MHz Fully-Integrated Buck Converter with Precise DCM Operation and Enhanced Light-Load Efficiency
Cheng Huang, The Hong Kong University of Science and Technology, Hong Kong

[SDC8] A 101 dB DR 1.1 mW Audio Delta-Sigma Modulator with Direct-Charge-Transfer Adder and Noise Shaping Enhancement
Tao Wang, Oregon State University, U.S.A

[SDC9] A 245 GHz, 2.6mW/Pixel Antenna-Less CMOS Imager with 0.7Fw/Hz Nep and 3.5m Backscattered Range
Adrian Tang, UCLA, U.S.A

[SDC10] A Multi-Phase Multi-Frequency Clock Generator Using Superharmonic Injection Locked Multipath Ring Oscillators As Frequency Dividers
Amr Hafez, UCLA, U.S.A

[SDC11] Performance and Side-Channel Attack Analysis of a Self Synchronous Montgomery Multiplier Processing Element for RSA in 40nm CMOS
Benjamin Devlin, The University of Tokyo, Japan

November 13, 2012 (Tuesday)

Open Ceremony

Time: 9:00 - 9:10

Room: 301

Welcome Speech

Time: 9:10 - 9:20

Room: 301

Plenary Talk 1

Time: 9:20 - 10:05

Room: 301

Expectations for the Semiconductor Technologies in EVs and HVs

Mr. Shoichi Sasaki

Prof., Keio Univ., Japan

Abstract: EVs and HVs will have a certain share in the future market place. To populate these vehicles, the semiconductor technologies will play a central role. And those technologies will be crucial for the quality of EVs and HVs.

As for the near term items, for example, the size and loss of inverter used in EVs and HVs are important because of its cost and electrical “fuel “ consumption.

To populate EV and HVs, cost will be the most crucial factor even in the future. The portion of battery cost will still be large compared to inverter and motor cost. Therefore there is a need of cutting the cost of batteries for EVs and HVs. To do so, there are some technologies undergoing. One is to redesign the circuit topology of traction motor system which can utilize the relatively inexpensive battery cells. And the other is to transmit the electrical energy from road to the vehicle without contact. These technologies are presented and expectations for the semiconductor technologies are explained.

Biography: He was born in 1949. He graduated from the University of Tokyo, and has B.S and

M.S. degree (Electrical Engineering). He joined Toyota Motor corp., and was mainly involved in the development of Electric and Hybrid vehicles. His main research field was the application of power electronics to the vehicle.

Through the contribution of the development of the Toyota Prius, and the related inventions, he was received the award of Ministry of Economy, Trade and Industry from the Japan Institute of Invention and Innovation (2004), and also received the Technical Award from The Japan Society of Mechanical Engineers (1998), IEEE 2010 Daniel E. Noble Award, IEEE 2011 Medal for Environmental and Safety Technologies. He is now interested in the system design for the advanced technology vehicles and systems. He is now the professor of Keio University Graduate School of System design and management.

Plenary Talk 2

Time: 10:05 - 10:50

Room: 301

Semiconductor Memory Scaling and Beyond

Dr. Sungjoo Hong

Senior VP, Head of R&D Division, SK hynix Inc., Korea

Abstract: Semiconductor is an indispensable component of modern electronic systems. The history of the semiconductor industry is namely the history of scaling, represented by the Moore’s Law describing that the number of transistors incorporated in a chip approximately doubles every 18 months, and the semiconductor industry has pursued the rule in practice. The semiconductor memory industry has even accelerated much faster scaling than the others, introducing doubling density almost every year, and which has consequently benefited consumers by advancing the mobile era. Two decades ago, the first storage product using Flash memory was 2MB in density, priced at $50/MB, but we

are enjoying 128GB with $1/GB today, and which is due to rapid scaling. Besides, every semiconductor memory company is facing the ultimate physical limit of scaling. Development of 1xnm technology for memory products requires controlling of 16 critical electrons for NAND Flash and an aspect ratio of capacitor of higher than 60 for DRAM. Natural question arising here is “What will be the next?”. As part of efforts to overcome those limits and grasp new opportunities, the paper will report on new memory technologies such as STT-RAM, ReRAM, and PCRAM, which are expected to meet such specifications as high density, low power, and high speed that the mobile era requires simultaneously.

Biography: Sungjoo Hong received BS in Physics at the Seoul National University (SNU) in 1985 and obtained MS and Ph.D. degree in Physics at the Korea Advanced Institute of Science Technology (KAIST) in 1987 and 1992, respectively. Then, he joined Hyundai Electronics Industries Co., Ltd in 1992 and the company had been renamed as Hynix Semiconductor Inc. (Currently SK hynix Inc.) in 2001. He became the head of Device and Process Integration Group of R&D division of Hynix Semiconductor Inc. in 2004. During his term of the head of the Device and Process Integration Group, he received the Korean Semiconductor Technology award (a Presidential citation) in 2006 for successful development of 512Mb DDR2 DRAM with 80nm that provided the world longest retention time performance and outstanding yield rate. In April of 2010, he was appointed as the head of R&D division of Hynix Semiconductor, now being in charge of the research and development of DRAM, NAND Flash, and new memory technologies such as Phase Change Memory, Spin-Transfer-Torque Memory and Resistance Memory. Additionally, he served as a member of JFE Technology Program Committee in the 2012 IEEE Symposium on VLSI Technology and Circuits.

Industry Session 1 Leading Edge SoCs and Memory

Time: 11:05 - 12:45

Room: 301

Co-Chairs : Stefan Rusu (Intel Corporation)

Shao-Jun Wei (Tsinghua University)

Industry 1-1 11:05-11:30

The First 22nm Ia Multi-CPU and GPU System-on-Chip Using Tri-Gate Transistors

Scott Siers, Satish Damaraju, Varghese George, Sanjeev Jahagirdar, Tanveer Khondker, Robert Milstrey, Sanjib Sarkar, Israel Stolero, Arun Subbiah (Intel Corporation, U.S.A)

Abstract: This paper describes the 22nm Intel® processor code name Ivy Bridge that integrates up to four high-performance Intel Architecture (IA) cores, a power/performance optimized graphics/media processing unit (GPU), as well as memory, PCIe*, and display controllers in the same die and is the first process using tri-gate transistors.

Industry 1-2 11:30-11:55

A 1.94m m², 38.17mW Dual VP8/H.264 Full-HD Encoder/Decoder LSI for Social Network Services (SNS) over Smart-Phones

Chi-Cheng Ju, Tsu-Ming Liu, Yi-Hau Chen, Kun-Bin Lee, Chia-Yun Cheng, Hsueh-Te Chao, Chih-Ming Wang, Tung-Hsing Wu, Tin-An Lin, Han-Liang Chou, Yu-Kun Lin, Cheng-Hung Liu, Wei-Cing Li, Yi-Hsin Huang, Tsung-Chuan Ma, Chun-Chia Chen, Hue-Min Lin, Min-Hao Chiu, Sheng-Jen Wang, Yung-Chang Chang, Chung-Hung Tsai (Mediatek Inc., Taiwan)

Abstract: A first dual-standard video encoder and decoder LSI providing VP8 (i.e. video format of WebM project for use of web's video) or H.264/AVC video recording and playback simultaneously is implemented with 28nm CMOS and occupies 1.94mm² of core area. Several area-efficient techniques are realized, leading to 43.6% of area reduction. A new rate control is designed to facilitate the adaptation of video data and frame rates for network services. Two fast algorithms and new bool encoder/decoder are proposed to enhance power efficiency. This chip consumes 28.15mW and 10.02mW of VP8 encoder and decoder average power for 1080p@30fps at 0.9V, respectively.

Industry 1-3 11:55-12:20

A High Performance 64Gb MLC NAND Flash Memory in 20nm CMOS Technology

Jinsu Park, Byoungsung You, Sangdon Lee, Kwangho Baek, Chunwoo Jeon, Taikyu Kang, Jae-Ho Lee, Minsu Kim, Daeil Choi, Jeawon Choi, Hyun Jeong, Jongwoo Kim, Eunseong Jang, Tae-Yun Kim, Changhyuk Lee, Jongki Nam, Bong-Seok Han, Kun- Ok Ahn, Ki-hyun Bae (SK hynix semiconductor, Korea)

Abstract: A 64Gb MLC NAND flash memory on 20nm CMOS technology has been developed. 135mm2 chip size is realized by 1-sided All-Bit-Line architecture and 128 cells in a string. 25MB/s program throughput with 2-bit/cell is achieved by reducing BL resistance and pump output loading using new BL control method and multi-split block decoder. This device also supports 400MB/s high speed interface.

Industry 1-4 12:20-12:45

The 3.0GHz 64-Thread SPARC T4 Processor

Jinuk Luke Shin, Robert Golla, Hongping Li, Sudesna Dash, Mary Jo Doherty, Greg Grohoski, Curtis McAllister（Oracle, U.S.A）

Abstract: The SPARC T4 processor introduces the next generation multi-threaded 64b S3 core and delivers up to 5x single thread performance improvement over its predecessor. The chip integrates eight cores, an 8-Bank 4MB L3 Cache, a 768GB/sec crossbar, a memory controller, PCI Gen2.0, 10G Ethernet and cache coherency controller with 2.4Tb/s high-speed I/Os. The dual-issue, out-of-order execution core features a 16-stage integer pipeline, extensive branch predictions, dynamic threading and enhanced cryptographic processing unit. The 406mm2 die is fabricated in TSMC’s 40nm process and contains 855million transistors and 2.6million flip-flops in a flip-chip ceramic package. Enhanced physical design methodologies and extensive power management features enable 3.0GHz operation in the same power envelope of its predecessor.

Industry Session 2　Energy Efficient Circuits for Emerging Applications

Time: 11:05 - 12:45

Room: 401 and 402

Co-Chairs : Ron Ho (Oracle)

Koji Kai (Panasonic)

Industry 2-1　11:05-11:30

On-Chip Single-Inductor Dual-Output DC-DC Boost Converter Having Dual Output/Input Modes for Utilizing External Power Transistor Drive and Micro-Computer Controlled MPPT

Yasunobu Nakase, Shinichi Hirose, Hiroshi Onoda, Yasuhiro Ido, Yoshiaki Shimizu, Tsukasa Oishi, Toshio Kumamoto, Toru Shimizu (Renasas Electronics Corporation, Japan)

Abstract: A compact on-chip SIDO DC-DC converter is proposed for portable battery or solar cell operating equipments. A current up to 30mA is supplied with own transistors in an internal drive mode and more than 100mA by utilizing external power transistors in an external drive mode. The efficiencies are 85% and 84% for each case. Cross regulation is solved by inserting an extra cycle before switching the outputs. For solar cell operation, any kind of maximum power point tracking (MPPT) is available with a clock calculated by a micro-computer. The converter exploits 99% of the expected power of a solar cell.

Industry 2-2　11:30-11:55

A Sub-400 fJ/Bit Thermal Tuner for Optical Resonant Ring Modulators in 40 nm CMOS

Philip Amberg, Eric Chang, Frankie Liu, Jon Lexau, Xuezhe Zheng, Guoliang Li, Ivan Shubin, John Cunningham, Ashok Krishnamoorthy, Ron Ho (Oracle Labs, U.A.S)

Abstract: Optical ring modulators are highly susceptible to external temperature noise and to self-heating from absorbed optical power. We mitigate both problems through circuit techniques. A control loop at the ring measures output power and controls a local heater to compensate for external temperature noise. A control loop at the receiver dynamically tracks DC variations to compensate for self-heating effects. The design has been implemented in a 40 nm TSMC technology.

Industry 2-3　11:55-12:20

A 0.5V 10MHz-to-100MHz 0.47μW/MHz Power Scalable Ad-PLL in 40nm CMOS

Yasuyuki Hiraku (Semiconductor Technology Academic Research Center, Japan), Isamu Hayashi (Semiconductor Technology Academic Research Center, Japan), Hayun Chung Keio University, Japan), Tadahiro Kuroda (Keio University, Japan), Hiroki Ishikuro (Keio University, Japan)

Abstract: This paper presents an ultra-low-voltage and low-power all-digital (AD) PLL. The AD-PLL consists of time-to-digital converter (TDC) combined 8-phase digitally controlled ring oscillator. The proposed AD-PLL eliminates a delay-line based TDC and suited for ultra-low-voltage and low-power operation in wide frequency range. The AD-PLL designed and fabricated in 40nm-CMOS technology operates with power consumption of 45.5μW at 0.5V power supply and 100MHz output frequency. The AD-PLL has power scalability from 10MHz to 100MHz with normalized power consumption lower than 0.47μW/MHz. The core area is 0.037mm².

Industry 2-4 12:20-12:45

A Low-Power 6.6-Gb/S Wireline Transceiver for Low-Cost FPGAs in 28nm CMOS

Jafar Savoj, Kenny Hsieh, Fu-Tai An, Michael Buckley, Jay Im, Xuewen Jiang, Anup Jose, Vassili Kireev, Kang Wei Lai, Hiep Pham, Didem Turker, Daniel Wu, Ken Chang

(Xilinx, Inc., U.S.A)

Abstract: This paper describes the design of a 0.5-6.6Gb/s fully-adaptive low-power quad transceiver embedded in state-of-the-art low-leakage 28nm CMOS FPGAs. The receiver front-end utilizes a wide input common-mode circuit and a 3-stage CTLE to remove the immediate post-cursor ISI. The CTLE is fully adaptive using sign-sign LMS algorithm and edge-based equalization. The transmitter utilizes a 3-tap FIR. The clocking network provides continuous operation range up to the maximum speed and incorporates two wide-range ring-based PLLs for enhanced clocking flexibility. The transceiver achieves BER < 10^{-15} at 6.6Gb/s over an 18dB loss channel. Power consumption is 129mW from 1.2V and 1V supplies.

Session 1 Analog Interfaces and Amplifiers

Time: 13:45 - 15:25

Room: 301

Co-Chairs : Tetsuya Hirose (Kobe University)

Shao-Jun Wei (University Macau)

1-1 13:45 – 14:10

An Energy-Efficient BBPLL-Based Force-Balanced Wheatstone Bridge Sensor-to-Digital Interface in 130nm CMOS

Jelle Van Rethy, Hans Danneels, Valentijn De Smedt, Wim Dehaene, Georges Gielen

(KU Leuven, Belgium)

Abstract: An energy-efficient time-based sensor interface in 130nm CMOS technology is presented for resistive sensors. A force-balanced Wheatstone bridge interface circuit with a highly-digital architecture is introduced, that combines low power consumption with improved overall PSRR. It has a noise-frequency-independent PSRR of 52dB, which is an improvement of 46dB over the voltage divider and of 26dB over the unbalanced Wheatstone bridge. The complete interface consumes only 124.5uW from a 1V supply with 10kHz input bandwidth and 10.4 bit resolution and 8.9 bit linearity, resulting in a state-of-the-art sensor Figure of Merit of 13.03 pJ/conversion.

1-2 14:10 – 14:35

An Integrated 12-V Electret Earphone Driver with Symmetric Cockcroft-Walton Pumping Topology for in-Ear Hearing Aids

Jen-Huan Tsai (National Tsing-Hua University, Taiwan), Chun-Yen Tseng (National Tsing-Hua University, Taiwan), Wei-Kai Tseng (National Tsing-Hua University, Taiwan), Tim K. Shia （Industrial Technology Research Institute, Taiwan), Po-Chiun Huang (National Tsing-Hua University, Taiwan)

Abstract: Electret-type earphone exhibits a great potential on in-ear hearing-aid applications for the low driving power requirement. However, to enable a static force for thin film¡¦s vibration, the input voltage swing has to be large. Instead of using HV technology, in this work we develop a 12-V bridge-type audio driving system by a standard 1.8-V 0.18-£gm CMOS. The system integrates two switched-capacitor voltage multipliers, asynchronous regulation loops, and switching-type high-voltage drivers. The proposed symmetric Cockcroft-Walton topology can use MOS thin gate as charging capacitors to save 50% on-chip capacitor area. With differential 12-V output, the maximum output driving current is above 400£gA. The peak sound pressure for single audio channel is above 80dB with the open-loop THD+N better than 0.6%.

1-3 14:35 – 15:00

A Chopper Stabilized Instrumentation Amplifier with Dual DC Cancellation Servo Loops for Biomedical Applications

Dong Han, Yuanjin Zheng（Nanyang Technological University, Singapore）

Abstract: A 1V 65nm 4.3iW differential difference amplifier based instrumentation amplifier for biomedical applications has been presented. To eliminate the DC baseline drift of the biomedical signals, novel and efficient fine-coarse DC offset cancellation servo loops have been proposed. Measured results show that the proposed instrumentation amplifier achieves 0.8ìVrms input referred noise from 0.5Hz to 200Hz with inband gain of 65.5V/V and noise efficiency factor of 5.7 for electrocardiograph signal monitoring.

1-4 15:00-15:25

A 20 µV/°C Digital Offset Compensation Technique for Comparators and Differential Amplifiers

Koon Lun Jackie Wong, Michael Le, Kwang Young Kim（Broadcom Corp, U.S.A）

Abstract: Digital offset compensation has been widely used for start-up calibration of analog ICs. It can be valuable in the design of an offset control circuit that has a minimal dependence on temperature. This eliminates the need to recalibrate the circuit during normal operation when the temperature may randomly fluctuate. This paper presents a gm-tracking technique used in an offset correction loop that drifts only 0.02 µV/C over a temperature range of 0°C to 100°C. Test circuits fabricated in a 40 nm CMOS technology confirm the performance of the proposed technique.

Session 2 Advanced Memory

Time: 13:45 - 15:50

Room: 406

Co-Chairs : Ken Takeuchi (Chuo University)

Meng-Fan Marvin Chang (National Tsing Hua University)

2-1 13:45 – 14:10

Adaptive Program Verify Scheme for Improving NAND Flash Memory Performance and Lifespan

Sang In Park (Samsung Electronics, Korea), Dongkun Shin (Sungkyunkwan University, Korea), Eui Gyu Han (Samsung Electronics, Korea)

Abstract: Since NAND flash memory program/erase (PE) cycling gradually degrades the reliability of memory cells, the redundancy of error-correction code (ECC) is determined so as to sufficiently ensure the PE cycling endurance at the end of memory lifetime. Therefore,

ECC redundancy is under-utilized when PE cycling number is relatively small at the early lifetime. Considering the variations on program speed and error rate depending on the program step pulse voltage in the incremental step pulse programming (ISPP), an adaptive program voltage scheme was proposed in order to improve program performance by exploiting the under-utilized ECC. However, the scheme missed the problem of increased voltage stress on memory cells at a large program step pulse voltage. The voltage stress will shorten the lifespan of flash memory devices. This paper proposes an adaptive verify voltage scheme, which trades the under-utilized ECC for improving program performance at the early lifetime of flash memory without decreasing the memory lifetime. The experiments with real NAND flash chips demonstrate up to 21% of program time improvement and 10% of lifetime improvement over the fixed verify voltage scheme.

2-2 14:10 – 14:35

An Efficient BCH Decoder with 124-Bit Correctability for Multi-Channel SSD Applications

Hung-Yuan Tsai, Chi-Heng Yang, Hsie-Chia Chang (National Chiao Tung University, Taiwan)

Abstract: This paper presents an low latency and area-efficient architecture for key equation solver (KES) in decoding BCH codes. We modify simplified inversionless Berlekamp-Massey (SiBM) algorithm by rescheduling initial value and removing the idle part during computation. Compared with the orinal SiBM algorithm, our new architecture implemented in BCH (18244, 16384;124) code saves 42% gate-count within t cycles. Moreover, the KES can simultaneously support 8-channel syndrome generators and Chien search logics to achieve 12.6Gb/s throughput under 198MHz operation frequency.

2-3 14:35 – 15:00

A 250-MHz 18-Mb Full Ternary Cam with Low Voltage Match Line Sense Amplifier in 65nm CMOS

Isamu Hayashi, Teruhiko Amano, Naoya Watanabe, Yuji Yano, Yasuto Kuroda, Masaya Shirata, Shizuo Morizane, Koji Hayano, Katsumi Dosaka, Koji Nii, Hideyuki Noda, Hiroyuki Kawai (Renesas Electronics Corporation, Japan)

Abstract: An 18Mb full ternary CAM with low voltage match line sense amplifier (LV-MA) is designed and fabricated in 65-nm bulk CMOS process. The die size is 99.06 mm2. The proposed LV-MA reduces the dynamic power consumption of match-lines to 33% compared to conventional one and realizes 42 % fast match-line sensing. The power consumption of fully paralleled search operation at 125-MHz is 5.4 W, which is 63% smaller than our previous work. At 1.0V typical supply voltage, the 250-MHz maximum search frequency is achieved.

2-4 15:00-15:25

An Embedded Energy Monitoring Circuit for a 128kbit SRAM with Body-Biased Sense-Amplifiers

Yildiz Sinangil, Anantha Chandrakasan (Massachusetts Institute of Technology, U.S.A)

Abstract: Embedded energy monitoring for critical components of a system can be used to enable better power management by capturing run time system conditions such as temperature and application load. In this work, an energy sensing circuit that provides digitally represented absolute energy per operation of a 128kbit SRAM is presented. Designed in 65nm low-power CMOS process, SRAMs can operate down to 370 mV. Energy sensing circuit consumes 16.7uW during sensing at 1.2V (only 0.28% of SRAM active power at the same voltage). For improved performance, SRAMs utilize body-biased PMOS input strong-arm type sense amplifiers that can achieve 45% tighter input offset distribution for only 3.47% total SRAM area overhead.

2-5 15:25-15:50

A 0.2V 16Kb 9T SRAM with Bitline Leakage Equalization and Cam-Assisted Write Performance Boosting for Improving Energy Efficiency

Bo Wang (NTU, Singapore), Truc Quynh Nguyen (NTU, Singapore),
Anh Tuan Do (NTU, Singapore), Jun Zhou (IME, Singapore), Minkyu Je (IME, Singapore),
Tony T. Kim (NTU, Singapore)

Abstract: An energy efficient 9T SRAM with bitline leakage equalization and Content -Addressable-Memory-assisted (CAM-assisted) performance boosting techniques is presented. The equalized read bitline leakage improves the read bitline swing by 6.8× at 0.2V. The proposed CAM-assisted boosting technique enhances the write performance of the multi-threshold CMOS (MTCMOS) SRAM array implemented with higher-Vth (HVT) devices. The inserted tiny CAM conceals the slow data development after data flipping, and therefore improves overall operating frequency in the near threshold region. A 16Kb SRAM test chip was fabricated in 65nm CMOS technology and showed the minimum energy of 0.33 pJ at 0.4V.

Session 3 TX RX Architecture and Building Blocks

Time: 13:45 - 15:50

Room: 401 and 402

Co-Chairs : Shuya Kishimoto (NEC)

Chun-Huat Heng (National University of Singapore)

3-1 13:45 – 14:10

A Low-power Reconfigurable Multi-Band Sliding-IF Transceiver for WBAN Hubs in 0.18um CMOS

Lingwei Zhang, Hanjun Jiang, Jianjun Wei, Jingjing Dong, Weitao Li, Jia Gao, Jianwei Cui, Fule Li, Baoyong Chi, Chun Zhang, Zhihua Wang (Tsinghua University, China)

Abstract: This paper reports a low-power transceiver for multi-band WBAN hubs. The transceiver involve a novel reconfigurable sliding-IF architecture which relaxes the frequency synthesizer tuning range from 80% to 25% for WBAN hub receivers to cover all the 400/900/2400 MHz frequency bands. Measurement results on the designed and fabricated multi-band transceiver shows that it has comparable or even better performance in terms of noise, linearity, RX sensitivity and power consumption compared to the single band transceivers in literature.

3-2 14:10 – 14:35

A 65nm CMOS, 1.5-mm2 Bluetooth Transceiver with Integrated Antenna Filter for Co-Existence with a WCDMA Transmitter

Mitsuyuki Ashida, Hideaki Majima, Yoshiaki Yoshihara, Mai Nozawa, Shoko Oda, Yoshinori Suzuki, Jun Deguchi, Hiroyuki Kobayashi, Shouhei Kousai, Ryuichi Fujimoto, Shinichiro Ishizuka, Tadashi Terada, Shunji Kawaguchi, Yasuo Unekawa, Mototsugu Hamada (Toshiba Corporation, Japan)

Abstract: This paper presents a fully integrated Bluetooth transceiver in a 65nm CMOS, which occupies 1.5mm² on the chip. It even integrates an antenna filter to reject blocker from the co-existing wireless system such as WCDMA and GSM. The frequency response of the integrated filter is controlled by an on-chip temperature monitor and achieves 30dB rejection over the entire WCDMA band-I of 1920 - 1980MHz and the temperature range from -40 to 80 degrees. From a 1.2V supply, it draws 53.1mA for RX with the sensitivity of -89.1dBm, and 65.3mA for TX with the output level of +4dBm.

3-3 14:35 – 15:00

A Power-Efficient All-Digital IR-UWB Transmitter with Configurable Pulse Shaping by Utilizing a Digital Amplitude Modulation Technique

Shuli Geng, Xican Chen, Woogeun Rhee (Tsinghua University, China), Jongjin Kim, Dongwook Kim (Samsung Advanced Institute of Technology, Korea), Zhihua Wang (Tsinghua University, China)

Abstract: This paper presents an all-digital IR-UWB transmitter with high energy efficiency and flexible pulse shaping for OOK modulation systems. A digital amplitude modulation (AM) technique is proposed to enable configurable pulse shaping with a single digital power amplifier (DPA) for low power design. The proposed transmitter implemented in 65nm CMOS achieves the maximum pulse energy of 3pJ/bit and occupies an active area of 0.08mm2, meeting the FCC spectrum mask in 3-5GHz UWB band with a PRF of 32MHz.

3-4 15:00-15:25

A 1.55mW Mixed-Signal Integrating Mixer for Direct Spectrum Estimation in 0.13um CMOS

Kevin Banovic, Anthony Chan Carusone (University of Toronto, Canada)

Abstract: A low power integrating mixer prototype chip for direct spectrum estimation is fabricated for opportunistic spectrum access, interference detection and built-in test applications. The integrating mixer consists of a folded architecture that combines mixing, current-domain windowing, and integration to implement the short-time Fourier transform (STFT). The design operates over a frequency range of 0.05-3GHz, consumes 1.55mW from a 1.2V supply and obtains a dynamic range (DR) of 24dB.

3-5 15:25-15:37

A 2.4 GHz CMOS Doherty Power Amplifier with Dynamic Biasing Scheme

Kohei Onizuka, Katsuyuki Ikeuchi, Shigehito Saigusa, Shoji Otaka (Toshiba Corporation, Japan)

Abstract: A watt-level, fully integrated 1:1 Doherty power amplifier with dynamic biasing scheme is demonstrated in 65 nm CMOS. The newly implemented dynamic biasing scheme for sub-PA solves the gain-linearity trade-off of the Doherty PA with enough back-off efficiency improvement, and protects the gate oxide of the sub-PA from over-voltage stress as well. The PA delivers 30.4 dBm of peak output power with maximum 6 points of PAE improvement compared with a class-B PA, and satisfies IEEE 802.11b and 11g spectrum masks at output power levels of 24.3 and 23.2 dBm, respectively, from supply voltage of 3.3 V.

3-6 15:37-15:50

A 3.0-W Wireless Power Receiver Circuit with 75-% Overall Efficiency

Young-Jin Moon, Yong-Seong Roh, Changsik Yoo (Hanyang University, Korea),

Dong-Zo Kim (Samsung Electronics, Korea)

Abstract: Resonant magnetic coupling is utilized to transfer 3.0-W power without wire. The received AC power is rectified by an active rectifier and then converted to the desired DC level by a switching DC-DC converter. The reverse leakage of the active rectifier is prevented by a delay locked loop (DLL) based delay compensation circuit. The overall power efficiency of the wireless power receiver implemented in a 0.35-um BCDMOS technology is 75-% when the resonant frequency of the magnetic resonator is 3.23-MHz.

Session 4 Energy Efficient Circuits and Techniques

Time: 13:45 - 15:50

Room: 403

Co-Chairs : Utpal Desai (Intel Corporation)

Keiichi Kushida (Toshiba)

4-1 13:45 – 14:10

A Built-in Self-Adjustment Scheme with Adaptive Body Bias Using P/N-Sensitive Digital Monitor Circuits

Islam A.K.M Mahfuzul, Norihiro Kamae, Tohru Ishihara, Hidetoshi Onodera

(Kyoto University, Japan)

Abstract: This paper proposes a built-in self-adjustment scheme to adjust pMOSFET and nMOSFET performances to their target values. Independent control of MOSFET performances can boost circuit performance without large leakage overhead. All-digital monitor circuits have been developed to detect pMOSFET and nMOSFET variations. The scheme has been fabricated in a 65 nm process. Measurement results from corner chips confirm the validity of the scheme. At 0.7 V operation, more than 50\% of circuit speed degradation has been recovered. The proposed scheme achieves 2.6 times leakage saving than the conventional critical path delay based scheme. The scheme is suitable for typical-case design and yield enhancement.

4-2 14:10 – 14:35

Green Semiconductor Technology with Ultra-Low Power on-Chip Charge-Recycling Power Circuit and System

Kazuhiro Ueda, Syunsuke Okura, Fukashi Morishita (Renesas Electronics Corporation, Japan), Kazutami Arimoto (Okayama Prefectural University, Japan), Leona Okamura , Tsutomu Yoshihara (Waseda University, Japan)

Abstract: For low power consumption, the charge-recycling system by reuse the energy between the two or more CPUs and the task scheduling technique for high efficiency are proposed. In this architecture, CPUs are divided into upper and lower load groups, and electrical charges are shared among the stacked CPUs and a tank capacitor. The LDOs improve the margin of accumulation of tank capacitor or task schedule operation. Although the power efficiency of the conventional system with a simple LDO is 44.4% at the maximum, that of the proposed charge-recycling system improves to 88.9%.

4-3 14:35 – 15:00

On-Chip Dual-Ring-Oscillator-Based Random-Fluctuation-Measurement Method for Detecting Lowest Voltage in Adaptive Voltage Scaling Systems

Goichi Ono, Misa Owa, Michiaki Nakayama, Yusuke Kanno (Hitachi, Ltd., Japan)

Abstract: On-chip dual-ring-oscillator sensor for detecting random device fluctuation within chip was developed with 40 nm CMOS technology. The sensor detects the Vth fluctuation due to the RDF with precision of 1 mV with }10% accuracy by calculating square sum of frequency difference of dual ring oscillators. This architecture can operate the sensor without any reference signals, and achieve small layout area compared with conventional analog sensor. The effect of RDF will be more remarkable in the case of low-voltage operation. Advanced AVS (including compensation for RDF) should be needed and this proposed sensor will act as a lowest voltage detector.

4-4 15:00-15:25

Monitoring Effective Supply Voltage Within Power Rails of Integrated Circuits

Takeshi Okumoto, Kumpei Yoshikawa, Makoto Nagata (Kobe University, Japan)

Abstract: An effective supply voltage monitor evaluates dynamic variation of (Vdd-Vss) within power rails of integrated circuits on a die. The monitor occupies an area of as small as 10.8 x 14.5 mm2 and is followed by backend digitizing circuits, both using 3.3 V thick oxide transistors in a 65 nm CMOS technology for covering all power domains from core circuits to peripheral I/O rings. A prototype demonstrates capturing of effective supply voltage waveforms in digital shift registers as well as in an array of analog comparators.

4-5 15:25-15:50

A 0.3-V All Digital Crystal-Less Clock Generator for Energy Harvester Applications

Jen-Chieh Liu, Wei-Chun Lee (Industrial Technology Research Institute, Taiwan), Hong-Yi Huang (National Taipei University, Taiwan),Kuo-Hsing Cheng (National Central University, Taiwan), Chao-Jen Huang, Yu-Wei Liang, Jia-Hung Peng, Yuan-Hua Chu (Industrial Technology Research Institute , Taiwan)

Abstract: A 0.3 V all digital crystal-less clock generator (CLCG) is presented for a hearing aid application. The all digital CLCG uses frequency difference between the ring oscillator and the digital controlled oscillator (DCO) to create a mapping table under process and temperature variations. The digital loop filter (DLF) adopts a successive-approximation register (SAR) algorithm for fast locking time. Thus, the worse case of locking time is 73 output cycles. For a hearing aid application, the core area of CLCG and hearing aid system are 62×78 μmm2 and 1900×1920 μmm2, respectively, in 65 nm CMOS process. The frequency accuracy is 12 MHz ±3.5% in four test chips. The power consumption is 5μW. In the period jitter, the RMS and peak-to-peak jitters are 326.4 ps and 2.05 ns, respectively. The frequency drift is smaller than ±4.3% from 0 to 100¢J. Thus, this work is also used for energy harvester applications.

Panel Discussion 1

Time: 16:05 - 17:45

Room: 301

Disruptive design for emerging technology after 3D Devices/Fin FET and beyond;

How can we make it ?

Organizer : Yung-Chou Peng, TSMC, Taiwan

Co-Organizer: Youngmin Shin, Samsung, Korea, South

Moderator : Toshiro Hiramoto, University of Tokyo, Japan

Panelists : Vinod Kariat, Cadence, USA

Seiichiro Yamaguchi, Fujitsu, Japan

Aaron Thean, IMEC, EU

Jae Cheol Son, Samsung, Korea, South

Jong-Ho Lee, Seoul National University, Korea, South

Philippe Magarshack, STM, France

Sally Liu, TSMC, Taiwan

Abstract: Conventional technology before N28 follows scaling rule, device behaviors are not far away from projection. Disruptive design could base on this projection to create disruptive design.

While technology enters into 3D/FinFET and beyond, device behaviors are complex and not similar as projection could be used before. Besides process and design flow enhancement, is there any design solution could be used to break through this limitation? A technology-matched disruptive design in time available becomes a challenge. Is the digital assisted analog the most possible approach? Or dose the analog assisted digital with 3D IC benefit more?

In this panel, each specialist will talk about their research, technical and practical challenges from different domains. And further we will be discussing approaches to break through the limitations on process, device behavior, design flow and co-optimization.

Panel Discussion 2

Time: 16:05 - 17:45

Room: 401 and 402

Challenge for Zero Stand-by Power Management

- Road-map to the "Normally-Off Computing" -

Organizer : Kazutami Arimoto, Okayama Prefecture University, Japan

Co-Organizer: Toru Shimizu, Renesas Electronics Corporation, Japan

Moderator : Hiroshi Nakamura, University of Tokyo, Japan

Panelists : Shinobu Fujita, Toshiba, Japan

Hoi Jun Yoo, KAIST, Korea, South

Masanori Hayashikoshi, Renesas, Japan

Hiroaki Takada, Nagoya University, Japan

Steven Bartling, TI, USA

Bert Gyselinckx, IMEC, EU

Shey-shi Lu, National Taiwan Unversity, Taiwan

Abstract: System level Green innovations, including Medical and Health-care Appliances, Smart City, Smart Car, and Smart Home etc. are expected to bring us more comfortable and higher-quality human life, but further energy efficiency is required for those systems to meet the expectation. “Normally-Off Computing” is believed as one of the most promising ways to satisfy the requirement. In Japan, Normally-Off Computing Project started at September 2011 under the supported of NEDO (New Energy and Industrial Technology Development Organization) and METI (Japanese Minister of Economy, Trade and Industry). Currently, The University of Tokyo, Renesas, Toshiba, and Rohm are leading this project in collaboration with 8 universities and national research institute to the goal of "Normally -Off Computing". Under the ideal normally-off computing, all the components of computer systems are completely powered off whenever they need not to operate, and hence Stand-by Power is not consumed at all. There remain, however, a lot of problems to be solved with

tight collaboration of wide range of design layers including device, circuits, architecture, software, and applications. In this panel, world leading engineers and researchers in these fields are invited and present their own visions on the expectation and challenges to the “Normally-Off Computing”.

November 14, 2012(Wednesday)

Plenary Talk 3

Time: 9:00 - 9:45

Room: 301

Integrated Circuits and Systems toward Smart Ubiquitous Patient-Centered Medical Environment

Dr. Ming-Fong Chen

Superintendent, National Taiwan University Hospital, Taiwan

Abstract: Integrated circuits and systems have emerged to play a critical role in supporting the patient-centered medical home (PCMH) model of health care delivery. PCMH model of care has been performed in National Taiwan University Hospital (NTUH), Taiwan. The wireless ECG monitoring devices capable of measuring nonlinear heart rate variability and providing GPS localization information help the cardiologists to better handle the emergency condition of heart failure. A multi-modal signaling processor has been integrated to address patient with acute coronary syndrome, ischemic stroke and subarachnoid hemorrhage and facilitate early detection of targeted events. Electro-sensing antibody probing system has also been realized for biomedical samples. The service package of Telecare center of NTUH is composed of synchronous transmission of biometrics, mutual telephone communication, and rapid decision-making support. By integrating the bio-medical MEMS sensors with silicon circuits into mobile phones, physiological signals and vital signs can be monitored at any place and any time. With the mobile phone as a personal medical information hub, the biometrics can be sent to cloud for real-time monitoring and further analysis.

Biography: Ming-Fong Chen obtained MD and PhD degrees in College of Medicine, National Taiwan University (NTU), Taipei, Taiwan in 1975 and 1990, respectively. He also obtained EMBA degree in College of Management, NTU in 2002. He completed his medical resident and cardiologist training at Department of Internal Medicine, NTU Hospital

from 1977 to 1981. He also received research fellowship in Department of Physiology and Biophysics at Georgetown University Medical Center, Washington, USA from 1991 to 1992. He got instructor, associate professor and professor of Internal Medicine at College of Medicine, NTU in 1989, 1990, and 1995, respectively. He became vice-superintendent, chief of Department of Internal Medicine and superintendent of NTU hospital in 2002, 2007 and 2008, respectively. He is fellow/member of many international societies (FACC, FESC, FACP etc). He also published many papers in world famous journals.

Plenary Talk 4

Time: 9:45 - 10:30

Room: 301

Technology Challenges and Opportunities for Ubiquitous Computing

Dr. Shekhar Borkar

Intel Fellow, Intel Corp. U.S.A

Abstract: Unprecedented transistor integration capacity will be available to make computing truly ubiquitous, but the energy consumption will be a major challenge. Compute energy can be reduced by employing near threshold voltage operation. However, data movement energy will become prohibitive. Software will have to be cognizant of data locality, with introspection for fine grain energy management. The entire stack has to participate in implementing resiliency. Such a holistic system approach will make computing truly ubiquitous.

Biography: Shekhar Borkar is an Intel Fellow, an IEEE Fellow, and Director of Extreme-scale technologies at Intel Corporation. Shekhar has been with Intel since 1981, worked on the 8051 family of microcontrollers, supercomputers, high performance, low power digital circuits research, and served as the principal investigator of the DARPA funded UHPC project. He has authored 83 peer reviewed publications in conferences, 31 papers in journals, 56 invited papers and keynotes, four book chapters, and has more than 50 patents issued. Shekhar served as the TPC chairman of VLSI Circuit Symposium in 2002, and as the conference chairman in 2004. Shekhar was an adjunct faculty at Oregon Graduate Institute, taught graduate course on VLSI design for more than 10 years. His research interests are low power, high performance digital circuits, high speed signaling, and system level optimization. Shekhar holds M.Sc. in Physics from University of Bombay in 1979, and MSEE from University of Notre Dame in 1981.

Session 5 High speed Transceivers and Building Blocks

Time: 10:45 - 12:50

Room: 301

Co-Chairs : Jun Terada (NTT)

Byungsub Kim (Postech)

5-1 10:45 – 11:10

A 20Gb/S Adaptive Duobinary Transceiver

Yu-Ming Ying, I-Ting Lee, Shen-Iuan Liu (National Taiwan University, Taiwan)

Abstract: A 20Gb/s adaptive duobinary transceiver has been realized in 90-nm CMOS technology. An adaptive transmitter is realized without a feedback channel. For the channels with different lengths, the tap coefficient of the transmitter is digitally adjusted to compensate the channel loss. It achieves a data rate of 20-Gb/s with a BER less than 10-12 over 16cm-FR4 board. The transmitter and receiver consume 81mW and 38mW from a 1.5V supply, respectively. For a 20-Gb/s PRBS of 2^7-1, the maximum length of FR4 channel 16cm is achieved. The measured peak-to-peak jitter of the recovered data is 13.78ps.

5-2 11:10 – 11:35

A 2.3-mW, 5-Gb/S Decision-Feedback Equalizing Receiver Front-End with Static-Power-Free Signal Summation and CDR-Based Precursor ISi Reduction

Seuk Son, Hanseok Kim, Myeong-Jae Park, Kyunghoon Kim, Jaeha Kim (Seoul National University, Korea)

Abstract: A 5Gb/s 2.3mW low-power decision feedback equalizer (DFE) is presented. For channel that has 15dB loss at 2.5GHz, it recovers 5Gb/s PRBS7 data with a horizontal eye opening of 0.66UI on experiment. TSMC 65nm low-power technology is used and the DFE occurs 60um x 60um.

5-3 11:35 – 12:00

A 24-Gb/S Source-Series Terminated Driver with Inductor Peaking in 28-nm CMOS

Kosuke Suzuki, Yasumoto Tomita, Hisakatsu Yamaguchi, Tszshing Cheung, Takuji Yamamoto, Hirotaka Tamura (Fujitsu Laboratories LTD, Japan)

Abstract: We designed and tested a 24-Gb/s source-series terminated (SST) driver in 28-nm CMOS. The driver is composed of four segments with different weights to achieve an adjustable tap-weight finite-impulse-response (FIR) filter. The driver consists of nine slices, each of which contains four driver units. Each driver unit has a minimum-sized output stage regardless of the tap weight to reduce the power consumption of the preceding pre-driver stages. Series inductors connected to the output terminal of the driver are used to form a pi-network circuit to enhance the bandwidth. The driver consumes 27.8 mW off a 0.85-V single supply. The total output jitter is 14.9 ps, which includes an input jitter of 11.1 ps. The core area is 330x 330um^2 with bumps.

5-4 12:00-12:25

A 5 Gb/S 1/4-Rate Clock and Data Recovery Circuit Using Dynamic Stepwise Bang-Bang Phase Detector

Yen-Long Lee, Soon-Jyh Chang, Rong-Sing Chu, Ying-Zu Lin, Yen-Chi Chen, Goh Jih Ren (National Cheng-Kung University, Taiwan), Chung-Ming Huang (Himax Technologies, Inc., Taiwan)

Abstract: This paper presents a 5-Gb/s 1/4-rate clock and data recovery (CDR) circuit. The proposed dynamic stepwise bang-bang phase detector comprises the advantage of linear and bang-bang phase detectors. The CDR adjusts the charge pump currents and the interpolation weight of phase interpolators according to the phase error between input data and feedback clock. This CDR consumes 16.8 mW from a 1.2-V supply and occupies an active area of 0.3 mm2. The measured peak-to-peak jitter and rms jitter of the recovered clock are 42.37 ps and 7.06 ps for a 5-Gb/s 27-1 PRBS, respectively.

5-5 12:25-12:50

A 0.1-1.5 GHz 8-Bit Inverter-Based Digital-to-Phase Converter Using Harmonic Rejection

Ming-Shuan Chen, Amr Amin Hafez, Chih-Kong Ken Yang (UCLA, U.S.A)

Abstract: In this paper, a 0.1-1.5 GHz 8-bit inverter-based digital-to-phase converter (DPC) is proposed. Conventional inverter-based DPC suffers from poor linearity and limited output frequency range. To mitigate the linearity problem and extend the output frequency range, we propose to use harmonic rejection (HR) filter to cancel out the 3rd- and 5th-order harmonics of the phase interpolated signal. The residual INL and DNL can be further eliminated by nonlinear interpolation technique. Designed and fabricated in 65-nm CMOS technology, the DPC demonstrates a maximum INL and DNL of 2.18 and 0.89 LSB while consumes a power of 4.3 mW and occupies 0.06 mm2 area.

Session 6 Nyquist-Rate ADCs

Time: 10:45 - 12:50

Room: 401

Co-Chairs : Tai-Cheng Lee (National Taiwan University)

Soon-Jyh Chang (National Cheng-Kung University)

6-1 10:45 – 11:10

A 1-GHz, 17.5-mW, 8-Bit Subranging ADC Using Offset-Cancelling Charge-Steering Amplifier

Kenichi Ohhata, Hiroyuki Takase, Minehiko Tateno, Mai Arita, Naohiro Imakake, Yuutou Yonemitsu (Kagoshima University, Japan)

Abstract: A 1-GHz, 17.5-mW, 8-bit subranging ADC was fabricated using 65-nm CMOS technology. We adopt an analog centric approach differing from the digital foreground calibration to reduce power dissipation. An offset cancelling charge-steering amplifier and the capacitive averaging technique effectively reduce the offset, noise, and power dissipation. Moreover, the compensation circuit for the noise current from the comparator can also reduce the power dissipation. The test chip fabricated in 65-nm digital CMOS technology shows a high-sampling rate of 1 GHz and low-power dissipation of 17.5 mW. This chip achieved the FOM of 118 fJ/conv.-step.

6-2 11:10 – 11:35

Inter-Stage Gain Error Self-Calibration of a 31.5fJ 10b 470MS/S Pipelined-SAR ADC

Jianyu Zhong, Yan Zhu, Sai Weng Sin, Seng-Pan U, Rui Paulo Martins (Univ. of Macau, China)

Abstract: This paper proposes an Inter-Stage Gain Error (ISGE) calibration method devoted to correct the residue gain errors induced by the parasitic effects, non-ideal op-amp gain and capacitor mismatch, and also the mismatches for supply-derived reference voltages between two stages for Pipeline SAR ADC. The calibration reuses the SAR ADC to estimate the overall inter-stage gain error and compensates it in the 2nd-stage DAC in 2 cycles, and it is implemented in a pipelined-SAR which achieves 10b 470 MS/s in 65nm CMOS with the FoM of 31.5fJ/conv.-step by consuming only 6% of the total ADC area (0.049mm²).

6-3 11:35 – 12:00

A 12-Bit 8.47-fJ/Conversion-Step 1-Ms/S SAR ADC Using Capacitor-Swapping Technique

Meng-Hsuan Wu, Yung-Hui Chung, Hung-Sung Li (MediaTek, Taiwan)

Abstract: This paper presents a 12-bit 1-MS/s SAR ADC incorporating a sampling capacitor-swapping technique. The proposed swapping technique effectively removes the capacitor-DAC middle-code transition error without needing large capacitor size for good capacitor matching. An on-the-fly programmable dynamic comparator is proposed for meeting fast comparison and low-noise requirements. The ADC was fabricated in 0.11 um CMOS. It consumes 16.47 uW at 0.9 V supply. Measured DNL and INL are 0.3 LSB and 0.56 LSB respectively. Measured SNR and SFDR are 67.5 dB and 87 dB respectively, equivalent to a FOM of 8.47 fJ/conversion-step.

6-4 12:00-12:25

A 40nm CMOS Full Asynchronous Nano-Watt SAR ADC with 98% Leakage Power Reduction by Boosted Self Power Gating

Ryota Sekimoto, Akira Shikata, Kentaro Yoshioka, Tadahiro Kuroda, Hiroki Ishikuro (Keio University, Japan)

Abstract: This paper presents an ultra low power and ultra low voltage SAR ADC. Full asynchronous operation and boosted self power gating are proposed to improve conversion accuracy and reduce static leakage power. Test chip fabricated in 40nm CMOS process has successfully reduced leakage power by 98% and it performs ENOB of 8.2bit and consumes only 0.65nW with 0.1kS/s at 0.5V. The power consumption is scalable up to 4MS/s and power supply range from 0.4 to 0.7V. The best figure of merit (FoM) of 5.2fJ/conversion-step was obtained with 20kS/s at 0.5V.

6-5 12:25-12:37

A 0.05mm² 0.6V 500Ks/s 14.3Fj/Conversion-Step 11-bit Two-Step Switching SAR ADC for 3-Dimensional Stacking CMOS Imager

Jin-Yi Lin, Hsin-Yuan Huang, Chih-Cheng Hsieh (National Tsing Hua University, Taiwan), Hung-I Chen (Industrial Technology Research Institute, Taiwan)

Abstract: This paper proposes a two-step switching SAR ADC architecture that greatly reduces the area and power consumption of the DAC network. The total number of unit capacitors of the proposed approach is only 64C. In addition, to reduce meta-stability at low-supply operation, a supply-boost technique of comparator is also employed. The prototype chip realized an 11-bit SAR ADC in a 0.18μm CMOS technology with an extremely small core area of 0.05mm2. With a single 0.6V supply voltage, the prototype consumes 5.02uW at 500kS/s, and achieves an ENOB of 9.45bit and a FoM of 14.34fJ/conversion-step, respectively.

6-6 12:37-12:50

A 9b 1GS/s 27mW Two-Stage Pipeline ADC in 45nm SOI-CMOS

Jorge Pernillo ,Michael Flynn (University of Michigan, U.S.A)

Abstract: A novel, 9b 1GS/s 2-stage pipeline ADC architecture enables high performance with a low-gain op-amp and poor accuracy in the sub-ADC comparators. A reduced MDAC gain of two relaxes the op-amp gain and bandwidth requirements by a factor of 5.7. Deliberate and random comparator mismatch set the trip-points in the 2nd stage flash sub-converter and decouples performance from matching requirements. Digital trimming of a delay chain eliminates mismatch in the sampling paths to provide a simple, low power alternative to a dedicated front-end SAH. The ADC achieves an ENOB of 7.4b at Nyquist, consumes 27mW from a 1.0V supply, yielding an FOM of 160fJ/conversion-step.

Session 7 Emerging Biomedical Circuits and Systems

Time: 10:45 - 12:50

Room: 402

Co-Chairs : Reiji Hattori (Kyusyu University)

Koji Kotani (Tohoku University)

7-1 10:45 – 11:10

Ultrasonic Imaging Front-End Design for CMUT: a 3-Level 30Vpp Pulse-Shaping Pulser with Improved Efficiency and a Noise-Optimized Receiver

Kailiang Chen, Anantha Chandrakasan, Charles Sodini (MIT, U.S.A)

Abstract: A four-channel analog front-end (AFE) transceiver chip for medical ultrasound imaging is demonstrated. The high voltage transmitter uses a 3-level pulse-shaping technique to deliver over 50% more acoustic power for the same power dissipation, compared to traditional methods. The design requires minimum off-chip components and is scalable for more channels. The receiver is implemented with a transimpedance amplifier (TIA) topology and is optimized for noise, bandwidth and power dissipation. Based on both acoustic and electrical measurements, we demonstrate the Transmitter (Tx) efficiency improvement, Tx beamformation and the pulse-echo response, revealing the system’s full functionality.

7-2 11:10 – 11:35

A Wirelessly Powered and Interrogated Blood Flow Monitoring Microsystem Fully Integrated with a Prosthetic Vascular Graft for Early Failure Detection

Jia Hao Cheong, Chee Keong Ho, Simon Sheung Yan Ng, Rui-Feng Xue (Institute of Microelectronics, Singapore), Hyouk-Kyu Cha(Seoul National University of Science and Technology, Korea), Pradeep Basappa Khannur, Xin Liu, Andreas Astuti Lee, Ferguson Noviar Endru (Institue of Microelectronics, Singapore), Woo-Tae Park (Seoul National University of Science and Technology, Korea), Li Shiah Lim, Cairan He, Minkyu Je (Institue of Microelectronics, Singapore)

Abstract: This paper presents an implantable blood flow monitoring microsystem embedded in a prosthetic graft for early graft failure detection. The microsystem consists of two MEMS pressure sensors, an inductively powered wireless sensor inter-face ASIC, two miniature coupling coils, and a flexible cable connecting them. The implantable microsystem is powered and configured by an external monitoring device using 13.56-MHz carrier frequency. The blood flow rate information is sensed in the form of an oscillation frequency and transmitted to the ex-ternal monitoring device through backscattering. The ASIC fabricated in 0.18-um CMOS process occupies a total area of 0.5 x 3.3 mm2 including pads and consumes a total power of 12.6 uW. With the high-efficiency design of coupling coils, rectifier and LDO, the wireless power link achieves an overall power efficiency of 2% through 5-cm-thick tissue. With the ultra low power consumption and high-efficiency power transfer, the ASIC can be powered by transmitting only 630-uW RF carrier from the external device. The measured performance of the blood flow monitoring microsystem demonstrates a 0.17-psi pressure resolution.

7-3 11:35 – 12:00

An Inductively Powered CMOS Multichannel Bionic Neural Link for Peripheral Nerve Function Restoration

Kian Ann Ng, Xu Liu, Jianming Zhao, Li Xuchuan, Shih-Cheng Yen (National University of Singapore,Singapore), Minkyu Je (Institute of Microelectronic, Singapore), Yong Ping Xu (National University of Singapore, Singapore), Ter Chyan Tan(National University Hospital, Singapore)

Abstract: This paper describes a inductively powered multi-channel bionic neural link (BNL) system-on-chip (SOC) for peripheral nerve function restoration. The BNL-SOC consists of 8 neural recording and 4 stimulation channels, and is implemented in a 0.35-μm CMOS technology. Full function of the BNL has been demonstrated with in-vivo animal experiments. The entire BNL SOC consumes 1.5mW and operates under a 3V supply with an external ±9V multichannel stimulation output driver.

7-4 12:00-12:25

100-Channel Wireless Neural Recording System with 54-Mb/S Data Link and 40%-Efficiency Power Link

Kuang-Wei Cheng (National Cheng-Kung University / Agency for Science, Technology and Research, Singapore), Xiaodan Zou, Jia Hao Cheong, Rui-Feng Xue, Zhiming Chen, Lei Yao, Hyouk-Kyu Cha, San Jeow Cheng, Peng Li(Agency for Science, Technology and Research, Singapore), Lei Liu (Agency for Science, Technology and Research / Nanyang Technological University, Singapore), Luis Andia, Chee Keong Ho, Ming-Yuan Cheng(Agency for Science, Technology and Research, Singapore), Zhu Duan (Agency for Science, Technology and Research / National University of Singapore, Singapore), Ramamoorthy Rajkumar (National University of Singapore, Singapore), Yuanjin Zheng, Wang Ling Goh Nanyang Technological University, Singapore), Yongxin Guo, Gavin Dawe (National University of Singapore, Singapore), Woo-Tae Park, Minkyu Je (Agency for Science, Technology and Research, Singapore)

Abstract: For real-time monitoring of brain activities, a high-data-rate, low-power, and highly mobile neural recording system is desirable. This paper presents a complete chipset for a 100-channel wireless neural recording system, which consists of 3 ICs - A neural interface (NI) IC and a wireless power RX and data TX IC for an implant unit (IU), and a wireless data RX IC for an external head unit (EHU). With a dual S/H NI architecture and a burst-mode (BM) wideband (WB) FSK TX, the IU achieves a 100-channel recording and wireless transmission at 54.24Mb/s while consuming only 6.6mW. Using power coupling with optimal resonant load transformation and high-efficiency rectifier and LDO circuits, the whole wireless power link achieves 40% efficiency over 1cm distance with 0.5cm tissue in between. The EHU needs to transmit the RF power lower than 30mW to operate the IU. The EHU is implemented using a crystal-less BM WB FSK RX consuming only 14.4mW at 27.12Mb/s.

7-5 12:25-12:37

A Dynamic Electrode Impedance Matched Acupuncture-Type Diagnosis System with Concurrent Feedback of Physiological Signals

Kiseok Song, Sunjoo Hong, Taehwan Roh, Unsoo Ha, Hoi-Jun Yoo (KAIST, Korea)

Abstract: A dynamic electrode impedance matched acupuncture-type diagnosis system is proposed for an active electro-acupuncture (EA) treatment with the concurrent feedback of physiological signals. The 4-channel ExG sensor front-end and the independent component analysis (ICA) processor, is used for the acquisition of pure ECG, EEG, and EMG signal when the EA stimulation is simultaneously applied to the human body. The EA stimulator front-end adopts both the large time constant (LTC) S/H current matching technique and the offset current regulation for the accurate charge balancing. As a result, it can achieve less than 10 nA DC offset current. There are 25 concentric circular electrodes in the bottom of the proposed system. The dynamic electrode impedance matching circuit monitors the stimulation voltage swing and optimizes the area of the stimulation electrodes and the sensing electrodes for the high CMRR. The proposed diagnosis IC of 5.0 mm x 5.0 mm is fabricated in 0.13 um RF CMOS technology, and dissipates only 3.6 mW from 1.2 V.

7-6 12:37-12:50

A Single-Chip Time-Interleaved 32-Channel Analog Beamformer for Ultrasound Medical Imaging

Ji-Yong Um, Jae-Hwan Kim, Eun-Woo Song, Yoon-Jee Kim, Jae-Yoon Sim, Hong-June Park (POSTECH, Korea)

Abstract: This paper proposes a single-chip time-interleaved 32-channel analog beamformer for ultrasound medical imaging. The proposed analog beamformer circuit consists of multiple sub analog beamformers which are time-interleaved for beamforming of multiple focal points on a scan line. Each sub analog beamformer executes beamforming for an assigned focal point on a scan line sequentially by sampling and summing the ultrasound echo signals of 32 channels. The proposed 32-channel analog beamformer circuit was fabricated in a single chip with an active area of 15.75 mm2 in a 0.13 um standard CMOS process. The total power consumption of the chip is 150 mW with a 1.2V supply. The delay resolution of the implemented analog beamformer circuit is 1/200 of the ultrasound carrier period. The analog beamformer operation was successfully verified through measurements by applying the emulated ultrasound echo signals taken from a commercial ultrasound imaging device through commercial DAC chips to the fabricated chip.

Session 8 Low-Power Digital Communication & Multimedia SoCs

Time: 10:45 - 12:50

Room: 403

Co-Chairs : Hirofumi Sumi (Sony)

Donghyun Kim (Samsung Techwin)

8-1 10:45 – 11:10

A 40 nm 535 Mbps Multiple Code-Rate Turbo Decoder Chip Using Reciprocal Dual Trellis

Chen Yang Lin, Cheng Chi Wong, Hsie Chia Chang (National Chiao Tung University, Taiwan)

Abstract: This paper implemented a multiple code-rate turbo decoder using reciprocal dual trellis and QPP interleaver in 40 nm CMOS. Two parallel SISO decoders are exploited to achieve higher throughput. The advantage of the reciprocal dual trellis in high code-rate decoder reduces not only the trellis complexity but also the size of sliding window. The proposed turbo decoder can support five code-rate codes, and the maximum throughput can achieve 535 Mbps with 218 mW power consumption. Consequently, the proposed turbo decoder can provide high throughput and better energy efficiency for communication systems requiring high code-rate schemes.

8-2 11:10 – 11:35

A (50,2,4) Nonbinary LDPC Convolutional Code Decoder Chip over Gf(256) in 90nm CMOS

Chia-Lung Lin, Chih-Lung Chen, Hsie-Chia Chang, Chen-Yi Lee (National Chiao Tung University, Taiwan)

Abstract: A memory-based (m_s=50,d_v=2,d_c=4) nonbinary LDPC convolutional code (NB-LDPC-CC) decoder over GF(256) with layered scheduling is presented. The proposed architecture-aware construction features fewer memory banks, low degree, and low period. To the best of our knowledge, this is the first architecture discussion and implementation for NB-LDPC-CC decoders. We optimized the architecture of message first-in-first-out (M-FIFO), check node unit, and variable node unit in terms of area and throughput. Jointly designing code and architecture, overall normalized area efficiency can be enhanced by more then six times with respect to decoders of nonbinary LDPC block codes (NB-LDPC BCs). After fabricated in 90nm CMOS, our prototype NB-LDPC-CC decoder chip can achieve maximum throughput of 22.8Mbps with frequency of 285MHz. The measured average power is 211mW at a typical operating voltage of 1.0V.

8-3 11:35 – 12:00

A Successive Cancellation Decoder ASIC for a 1024-Bit Polar Code in 180nm CMOS

Anadi Mishra (École Polytechnique Fédérale de Lausanne, Switzerland), Alexandre Raymond (McGill University, Canada), Luca Amaru (École Polytechnique Fédérale de Lausanne, Switzerland), Gabi Sarkis (McGill University, Canada), Camille Leroux (}Institut Polytechnique de Bordeaux, France), Pascal Meinerzhagen, Andreas Burg(École Polytechnique Fédérale de Lausanne, Switzerland), Warren Gross (McGill University, Canada)

Abstract: This paper presents the first ASIC implementation of a successive cancellation (SC) decoder for polar codes. The implemented ASIC relies on a semi-parallel architecture where processing resources are reused to achieve good hardware efficiency. A speculative decoding technique is employed to increases throughput by 25% at the cost of very limited added complexity. The resulting architecture is implemented in a 180nm technology. The fabricated chip can be clocked at 150 MHz and uses 183k gates. It was verified using an FPGA testing setup and provides reference for the true silicon complexity of SC decoders for polar codes.

8-4 12:00-12:25

Crisp-II: Coarse-Grained Reconfigurable Image Stream Processor for Image-Processing and Intelligent Operations in QFHD Video Cameras

Teng-Yuan Cheng, Liang-Gee Chen, Shao-Yi Chien (National Taiwan University, Taiwan)

Abstract: A 372.3mW coarse-grained reconfigurable image stream processor, CRISP-II, for image-processing and intelligent operations is implemented in TSMC 90nm low-power technology with a core size of 15.21mm2. With the proposed multi-stream mode unified protocol, hierarchical ring architecture, and adaptive computing engine, CRISP-II is able to solve the emerging scalability and flexibility problems. It could execute several advanced operations efficiently, like high-dynamic-imaging and face detection. Compared with other state-of-the-art processors, CRISP-II achieves 8.42 times power efficiency than the highly parallel SIMD processor, and meets the real-time requirement of video cameras with QFHD (3840x2160) resolution.

8-5 12:25-12:37

A Dynamic Resource Controller with Network-on-Chip for a 10.5nJ/Pixel Object Recognition Processor

Jinwook Oh, Injoon Hong, Gyeonghoon Kim, Junyoung Park, Hoi-Jun Yoo

KAIST, Korea, South

Abstract: This paper presents a dynamic resource controller (DRC) with network-on-chip (NoC) for an energy-efficient multi-core processor. A total 21 cores in 5 local voltage/frequency islands (VFIs) can be controlled by dynamic resource management (DRM) with the proposed workload-utilization product based prediction model. And a 0.31mm2 compact 8x8 NoC switch is designed to reduce unnecessary ~24% power dissipation of each VFI by adopting DVFS and the bandwidth regulation. As a result, thanks to 42% reduction of power-delay product by DRM-based NoC architecture, the 32 mm2 multi-core processor, fabricated 0.13um CMOS process, achieves 10.5nJ/pixel efficiency, 3.54x improvement compared to state-of-the-art object recognition processors.

8-6 12:37-12:50

An 800Mhz Cryptographic Pairing Processor in 65nm CMOS

Yang Li, Jun Han, Shuai Wang, Dabing Fang, Xiaoyang Zeng (Fudan University, China)

Abstract: Pairings are attractive and competitive cryptographic primitives for establishing various novel and powerful information security schemes. An efficient implementation of pairings is usually critical for realizing a cryptographic scheme practically. This paper presents a high-performance pairing processor with a new combined Montgomery multiplier which implements the fundamental operations of Fp2 multiplication efficiently. The processor is fabricated in TSMC 65nm CMOS process. The chip achieves 800MHz (1.2V) with 266.5mW power consumption and a core area of 2.51mm2, and computes an optimal Ate pairing (254-bit curve) in 0.64ms.

Session 9 Power Management ICs

Time: 13:50 - 15:55

Room: 301

Co-Chairs : Seung-Tak Ryu (KAIST)

Po-Chiun Huang (National Tsing Hua University)

9-1 13:50 – 14:15

A Package Bondwire Based 80% Efficiency 80MHz Fully-Integrated Buck Converter with Precise DCM Operation and Enhanced Light-Load Efficiency

Cheng Huang, Philip Mok (The Hong Kong University of Science and Technology, Hong Kong)

Abstract: An 80MHz fixed frequency PWM fully-integrated area-efficient buck converter utilizing standard package bondwire as power inductor with enhanced light-load efficiency is presented which occupies 1.2mm2 in 0.13um CMOS. Package bondwire instead of on-chip spiral metal or special spiral bondwire is utilized as power inductor. Two negative feedback loops are proposed as NMOS gate-drive controller to introduce Adaptive Dead-Time (ADT) and precise Discontinuous-Conduction-Mode (DCM) operation with self-eliminated reverse current at high frequency, which frees the accuracy requirement of the package bondwire inductor and boosts up the light-load efficiency over 72% at 10mA while reaches 80% at 270mA with a 6.7nH inductor. 8 times efficiency improvement at 10mA is observed comparing to the situation with all the proposed function disabled. Converters with different package bondwire inductors from 3nH to 10nH are tested to verify the robustness.

9-2 14:15 – 14:40

A Single-Inductor Dual-Output Converter with Switchable Digital-or-Analog Low-Dropout Regulator for Ripple Suppression and High Efficiency Operation

Yu-Huei Lee, Wei-Chung Chen, Chao-Chang Chiu, Shen-Yu Peng, Kuan-Yu Chu, Ke-Horng Chen (National Chiao Tung University, Taiwan), Ying-Hsi Lin, Tsung-Yen Tsai, Chen-Chih Huang, Chao-Cheng Lee (Realtek Semiconductor Corporation, Taiwan), Yu-Wen Chen (Vanguard International Semiconductor Corp., Taiwan), Chao-Chiun Liang, Chang-An Ho,Tun-Hao Yu (Industrial Technology Research Institute, Taiwan)

Abstract: A single-inductor dual-output (SIDO) converter with the switchable digital-or-analog (D/A) low-dropout (LDO) regulator achieves an analog dynamic voltage scaling (ADVS) function for ripple suppression and high efficiency in system-on-a-chip (SoC). The ADVS function helps dynamically adjust the dropout voltage of the switchable D/A LDO regulator with analog operation for ripple suppression according to the load current. On other hand, the switchable D/A LDO regulator activates the digital operation for high efficiency at light loads since the dropout voltage of the LDO regulator can be further reduced. Besides, the bidirectional asynchronous signal pipeline (BASP) can realize the 50nA quiescent current in digital LDO regulator. This chip was fabricated by the 40 nm CMOS process. Experimental results demonstrate the switchable LDO regulator operation with the peak efficiency of 92% and the 7 mV output voltage ripple at 200 mA load because of the ripple suppression. The efficiency can be kept higher than 83% even the load current is 1 mA.

9-3 14:40 – 15:05

Automatic Loading Detection (ALD) Technique for 92% High Efficiency Interleaving Power Factor Correction (PFC) over a Wide Output Power of 180W

Jen-Chieh Tsai, Chun-Yen Chen, Yi-Ting Chen, Chia-Lung Ni, Yi-Ping Su, Ke-Horng Chen (National Chiao Tung University, Taiwan), Yu-Wen Chen (Vanguard International Semiconductor Corp., Taiwan), Chao-Chiun Liang, Chang-An Ho, Tun-Hao Yu (Industrial Technology Research Institute, Taiwan)

Abstract: the proposed automatic loading detection (ALD) technique keeps high efficiency in interleaving power factor correction (PFC) over a wide load range. With the advantages of small input/output filter and output ripple in the interleaving mechanism, the improved efficiency by the ALD technique at light loads due to reduced switching loss can be widely used in the adapter of portable electronics. The ALD technique can calculate the power by the detection of peak input voltage to reduce the switching loss since the slave channel can be completely turned off for power saving at light loads. Therefore, the boundary control mode (BCM) control can simultaneously provide high power and keep high conversion efficiency both at light and heavy loads. The highly integrated PFC controller fabricated in TSMC 800V UHV process shows high efficiency of 92% over a wide output power of 180 W.

9-4 15:05-15:30

A Chip-Area-Efficient CMOS Low-Dropout Regulator Using Wide-Swing Voltage Buffer with Parabolic Adaptive Biasing for Portable Applications

Yonggen Liu, Chenchang Zhan, Lin Cheng, Wing-Hung Ki (The Hong Kong University of Science and Technology, Hong Kong)

Abstract: In this paper, a chip-area-efficient CMOS low-dropout regulator (LDR) based on a wide-swing voltage buffer is proposed for battery-powered portable applications. To accommodate for the Li-Ion battery voltage range, high-voltage devices are used as the power transistor and in the error amplifier. By using a low-threshold PMOS with a novel parabolic adaptive biasing technique in the buffer, the voltage overhead is dramatically reduced, allowing a small-sized power transistor that works in the linear region at heavy load to be used while still maintaining a large load range and a tight regulation. The operation principle and the stability issue without using any compensation capacitors are discussed. The proposed LDR has been fabricated in a standard 0.13-μm CMOS process. With 0.2V dropout and 200mA maximum load current, the measured load regulation is 85μV/mA while the occupied active chip area is only 0.045mm2.

9-5 15:30-15:55

A Low-Power and Low-Cost Digitally-Controlled Boost Led Driver IC for Backlights

Tak-Jun Oh, Ara Cho, Seok-Lip Ki, In-Chul Hwang (Kangwon National University, Korea)

Abstract: This paper describes a digitally-controlled boost converter based LED driver IC for LED backlighting. We propose a new Analog-to-Digital Converter (ADC) with programmable quantization step and Lowest Voltage Selector (LVS) base on the time-digitizing circuits for Continuous Conduction Mode (CCM) operation of the boost converter. The proposed ADC and LVS can be fully implemented on a small silicon area and is suitable low power controller for LED driver IC. The 2-channel LED driver IC fabricated on a 0.35mm2 BCD process occupies the active area 1.35mm2 including the entire compensation filter. The maximum efficiency is measured to be 90% or more and the start-up settling time is within 800us.

Session 10 Oversampling ADCs

Time: 13:50 - 15:55

Room: 401

Co-Chairs : Takeshi Yoshida (Hiroshima University)

Zhongyuan Chang (Shanghai Belling Co.)

10-1 13:50 – 14:15

A 1.2V 64fJ/Conversion-Step Continuous-Time Sigma-Delta Modulator Using Asynchronous SAR Quantizer and Digital Delta-Sigma Truncator

Hung-Chieh Tsai, Chi-Lun Lo, Chen-Yen Ho, Yu-Hsin Lin (MediaTek Inc., Taiwan)

Abstract: A 3rd-order single-loop continuous time sigma-delta modulator (CTSDM) with 6-bit asynchronous SAR quantizer and digital delta-sigma truncator for WCDMA/GSM/EDGE cellular systems is presented. The proposed asynchronous SAR based quantizer reduces the area and power dramatically with the help of digital truncation technique. In addition, the modulator incorporating the proposed operational amplifiers (op-amp) with ac coupled push-pull stage is to improve the high frequency driving capability. The modulator sampling at 65MHz achieves 83.4dB dynamic range (DR) and 80/79.6dB peak SNR/SNDR with 1.92MHz bandwidth (BW) in WCDMA mode. In GSM/EDGE mode, the DR is 96.2 dB. Implemented in 40nm CMOS, the modulator occupies 0.051mm2 and consumes 1.91mW from a 1.2V supply. A 64fJ/conversion figure of merit (FOM) is achieved.

10-2 14:15 – 14:40

A 7.5 mW 9 MHz CT Delta-Sigma Modulator in 65 nm CMOS with 69 dB SNDR and Reduced Sensitivity to Loop Delay Variations

Mattias Andersson (Lund University, Sweden), Martin Anderson, Lars Sundström (Ericsson AB, Sweden), Pietro Andreani (Lund University, Sweden)

Abstract: This paper presents a 3rd-order, 3-bit continuous time (CT) $\Delta\Sigma$ modulator for an LTE radio receiver. By adopting a return-to-zero (RZ) pulse in the innermost DAC, the modulator shows a reduced sensitivity to loop-delay variations, and the additional loop delay compensation usually needed in CT modulators can be omitted. The modulator has been implemented in a 65nm CMOS process, where it occupies an area of 0.2mmx0.4mm. It achieves an SNR of 71dB and an SNDR of 69dB over a 9MHz bandwidth with an oversampling ratio of 16, while consuming 7.5mW from a 1.2V supply.

10-3 14:40 – 15:05

A 101 dB DR 1.1 mW Audio Delta-Sigma Modulator with Direct-Charge-Transfer Adder and Noise Shaping Enhancement

Tao Wang, Wei Li (Oregon State University, U.S.A), Hirokazu Yoshizawa (Saitama Institute of Technology, Japan), Mehmet Aslan(Texas Instruments, U.S.A), Gabor C. Temes ((Oregon State University, U.S.A)

Abstract: A low-power audio delta-sigma modulator (DSM) is presented. Two new techniques are proposed to reduce the overall power dissipation of the modulator: a power-efficient direct -charge-transfer adder is employed, and noise-shaping enhancement is implemented by feeding the differentiated quantization noise to the input of the second integrator. The measured power dissipation is 1.1 mW, the dynamic range is 101.3 dB, the spur-free dynamic range is 112 dB and the signal-to-noise-plus-distortion ratio is 99.3 dB. The power efficiency of this design is among the best in DSMs with high (over 15) ENOBs.

10-4 15:05-15:30

A 0.8 V 80.3 dB SNDR Stage-Shared Delta-Sigma Modulator with Chopper-Embedded Switched-Opamp for Biomedical Application

Chuan-Hung Hsiao, Wei-Lin Chen, Chih-Cheng Hsieh (National Tsing Hua University, Taiwan)

Abstract: This paper presents a one-bit third-order discrete-time sigma-delta modulator (DT-SDM) using standard CMOS 0.18-um process. Switched-opamp (SO) technique was utilized to deal with low supply constraint of sub-1-V operation. The cascade of resonators with distributed feed forward (CRFF) architecture reduces the signal swing of integrators, alleviating operation. A novel chopper-embedded OTA implemented in the first stage effectively eases the impact of component mismatches and suppresses the 1/f noise. The second and third stages share a single OTA to save the area and power budget. Operated at 0.8-V supply voltage, the proposed modulator achieves 80.3 dB peak SNDR with a 3 kHz sinusoid input over a signal bandwidth of 10kHz with an OSR of 128 at sampling frequency of 2.56 MHz and a power dissipation of 54 uW. The result Figure –of-Merits (FoMs) are 299 fJ/step and 319 fJ/step at 0.7-V and 0.8-V supply respectively.

10-5 15:30-15:55

A 22.4uW 80dB SNDR Sigma-Delta Modulator with Passive Analog Adder and SAR Quantizer for EMG Application

Zhijie Chen, Yang Jiang, Chenyan Cai, He-Gong Wei, Sai-Wen Sin, Seng-Pan U (University of Macau, Macau), Zhihua Wang (Tsinghua University, China), Rui Paulo Martins (University of Macau, Macau)

Abstract: A Feed-Forward (FF) multi-bit sigma-delta modulator with passive analog adder and 4-bit Successive Approximation (SA) quantizer is presented. The modulator covers the 10KHz bandwidth according to electromyography application. The design utilizes the same DAC array of the SAR quantizer to realize analog summation for the FF signal, which significantly reduces the power dissipation and the silicon area. The modulator operates at 1MS/s with 1V supply. The prototype chip implemented in 65nm CMOS achieves 80dB SNDR and 81dB DR with 22.4μW power consumption. The Figure of Merit (FoM) is 0.13 pJ/conv.-step.

Session 11 Millimeter-Wave Circuits and Systems

Time: 13:50 - 15:55

Room: 402

Co-Chairs : Minoru Fujishima (Hiroshima University)

Huei Wang (National Taiwan University)

11-1 13:50 – 14:15

A 245 GHz, 2.6mW/Pixel Antenna-Less CMOS Imager with 0.7fW/Hz05 Nep and 3.5m Backscattered Range

Adrian Tang, Hao Wu, Frank Chang (UCLA, U.S.A)

Abstract: An Antenna-less Regenerative Receiver (ARR) with sub- fW/Hz noise equivalent power (NEP) and 10 GV/W responsivity for reflective imaging applications is presented. The proposed ARR eliminates the need for a separate antenna can capture reflective images of plastic replica weapons at stand-off distances up to 3.5m with 30º off-incidence angle. Operating at 245 GHz, the ARR consumes only 0.036 mm2 of silicon area and 2.6 mW/pixel of power in 40nm CMOS technology.

11-2 14:15 – 14:40

A 34.8%-PAE CMOS Transmitter Frontend for 24-GHz FMCW Radar Applications

Huan-Sheng Chen, Liang-Hung Lu (National Taiwan University, Taiwan)

Abstract: A high-efficiency transmitter frontend circuit suitable for 24-GHz frequency-modulated continuous-wave (FMCW) radar applications is presented in this paper. In addition to the power amplifier (PA) stage, a voltage-controlled oscillator (VCO) is incorporated in the frontend for frequency modulation while a VCO buffer and a driving amplifier (DA) are utilized to provide an adequate driving level and reverse isolation. To take full advantage of the power available from the transistors, both the PA and DA stages are matched to the near-optimum impedances suggested by the load-pull simulation. Moreover, a positive-feedback technique is employed in the PA design for further efficiency enhancement. The proposed circuit is fabricated in a standard 90-nm CMOS process. Operated at a supply voltage of 1.2-V, the 24-GHz frontend demonstrates a peak power-added efficiency (PAE) of 34.8% with a peak output power of 16.3 dBm.

11-3 14:40 – 15:05

A 0.7V-to-1.0V 10.1 dBm-to-13.2 dBm 60-GHz Power Amplifier Using Digitally-Assisted LDO Considering HCI Issues

Rui Wu, Yuuki Tsukui, Ryo Minami, Kenichi Okada, Akira Matsuzawa (Tokyo Institute of Technology, Japan)

Abstract: A 60-GHz power amplifier (PA) with consideration of hot-carrier-induced (HCI) degradation is presented. The supply voltage of the last stage of the PA (V_{PA}) is dynamically controlled by an on-chip digitally-assisted low drop-out voltage regulator to alleviate HCI effects. The PA is fabricated in a standard 65-nm CMOS process with a core area of 0.21mm^2, which provides a saturation power of 10.1dBm to 13.2dBm with a peak power-added efficiency of 8.1% to 15.0% for V_{PA} varying from 0.7V to 1.0V at 60 GHz, respectively.

11-4 15:05-15:30

A 60 GHz Wideband Active Balun Using Magnitude and Phase Concurrent Correction Technique in 65nm CMOS

Shuo-Chun Chou, Fu-Chien Huang, Chorng-Kuang Wang (National Taiwan University, Taiwan)

Abstract: A wideband magnitude and phase concurrent correction technique (MPCCT) is proposed in this paper. The MPCT can concurrently correct the gain and phase imbalances between the differential signals of an active balun. This technique employs positive feedback and negative feedback as correction circuits. The two feedback loops redistribute the gain and phase imbalances into the differential outputs equally. The balun using MPCT has the measured maximum gain 6.1dB at 59GHz while the gain and phase imbalances are 0.14 dB and 0.7° respectively. The power consumption is 11.6mW with 1V supply voltage.

11-5 15:30-15:42

A 60GHz VCO with 25.8% Tuning Range by Switching Return-Path in 65nm CMOS

Wei Fei, Hao Yu, Kiat Seng Yeo, Wei Meng Lim (Nanyang Technological University, Singapore)

Abstract: This paper presents a novel inductive tuning method for 60GHz voltage controlled oscillator (VCO) design. A new inductor-loaded transformer is proposed by configuring different current return-paths in the secondary coil of a transformer. Different from previously published inductive tuning methods, the proposed topology can achieve a multi-band, wide tuning range within compact area using only one transformer. A 60GHz VCO is implemented at 65nm CMOS process for demonstration. The measured oscillation frequency can vary from 51.9GHz to 67.3GHz, which covers the full 60GHz band and provides a wide frequency tuning range of 25.8%.

11-6 15:42-15:55

A 60GHz CMOS Rectifier with -27.5dBm Sensitivity for mm-Wave Power Detection

Shusuke Kawai, Toshiya Mitomo, Shigehito Saigusa (Toshiba Corporation , Japan)

Abstract: A CMOS rectifier that converts 60 GHz signal to DC voltage is presented for millimeter-Wave (mm-Wave) power detection. The sensitivity of the rectifier is -27.5 dBm, which is 22 dB higher than in the previous work. The optimization method for the rectifier is proposed considering the power matching design and loss of the passive devices at 60GHz. According to the proposed method, the number of stage should be decreased because the stacked structure that is often used at frequency of several GHz doesn ft increase the sensitivity in the case of 60GHz. The loss of the passive devices is minimized by adopting the proposed optimization method.

Session 12 Clock Generation and Timing Circuits

Time: 13:50 - 15:55

Room: 403

Co-Chairs : Johngsun Kim (Hongik University)

Kibune Masaya (Fujitsu Laboratries)

12-1 13:50 – 14:15

A Spread Spectrum Clock Generator Using Phase/Frequency Boosting with a Peak Power Reduction 14.9dB, RMS Jitter 1.40ps and Power 4.8mW/GHz for USB 3.0

Seong-Hwan Jeon, Young-Ho Choi, Byung-Sub Kim, Jae-Yoon Sim, Hong-June Park (Pohang University of Science and Technology, Korea)

Abstract: A 2.5 GHz spread spectrum clock generator (SSCG) is proposed for USB 3.0. The low jitter is achieved by setting the normal loop bandwidth to an optimum value, considering both the VCO noise and the quantization noise of $\Delta\Sigma$ modulator. A large peak power reduction is achieved by maintaining a sharp triangular frequency profile through phase/frequency boosting when the phase error between two inputs of PFD exceeds a limit ($2\pi \times$ 2/9 rad). The peak power reduction and the RMS jitter are measured to be -14.9dB at the RBW of 100 KHz and 1.40ps, respectively. The chip area is 0.34mm x 0.36mm in a 0.13um process.

12-2 14:15 – 14:40

A Multi-Phase Multi-Frequency Clock Generator Using Superharmonic Injection Locked Multipath Ring Oscillators as Frequency Dividers

Amr Hafez, Ming-Shuan Chen, Chih-Kong Ken Yang (UCLA, U.S.A)

Abstract: A phase-locked loop providing multiphase clocks at 12-GHz and its subdivisions is presented. A quadrature VCO with low supply sensitivity is used. Frequency division is achieved using superharmonic injection-locked multipath ring oscillators to extend the maximum division frequency of latch-based dividers without using peaking inductors. A low mismatch charge pump reduces the reference spur level to a worst case of -74 dBc. The phase locked loop is fabricated in 65-nm CMOS. It operates in a frequency band between 7.92-12.11 GHz. The measured phase noise, random jitter, and power consumption at 12.08 GHz output frequency are -127.5 dBc/Hz at 10 MHz offset, 251 fs-rms, and 46.6 mW, respectively.

12-3 14:40 – 15:05

A High-Resolution Wide-Range Dual-Loop Digital Delay-Locked Loop Using a Hybrid Search Algorithm

Sangwoo Han, Jongsun Kim (Hongik University, Korea)

Abstract: This paper presents a dual-loop digital delay-locked loop (DLL) for high-speed DRAM applications. The dual-loop architecture using a hybrid (binary + sequential) search algorithm is proposed to achieve both wide-range operation and high delay resolution while maintaining the closed-loop property that allows for tracking of PVT variations. A new phase-interpolation range selector (PIRS) and a variable successive approximation register (VSAR) algorithm are adopted to resolve the boundary switching and harmonic locking problems of conventional digital DLLs. The proposed digital DLL, implemented in a 0.18-μm CMOS process, occupies an active area of only 0.19mm2 and operates over a wide frequency range of 0.15–1.5 GHz. The DLL also dissipates a power of 11.3 mW from a 1.8 V supply at 1 GHz. The measured peak-to-peak output clock jitter is 24 ps with an input clock jitter of 7.5 ps at 1.5 GHz. The delay resolution is only 2.2 ps

12-4 15:05-15:30

An All-Digital Phase-Locked Loop with Dynamic Phase Control for Fast Locking

Yun-Chen Chuang, Sung-Lin Tsai, Cheng-En Liu, Tsung-Hsien Lin (National Taiwan University, Taiwan)

Abstract: An all-digital phase-locked loop (ADPLL) featuring a dynamic phase compensation to accomplish fast-locking is reported. When a frequency-hopping event occurs, the compensation scheme implemented in both frequency and phase domain facilitates agile frequency settling. The phase error is monitored by an auxiliary time-to-digital converter (TDC) to control the divider ratio which directly modulates the frequency of the digital-controlled oscillator (DCO) through an integral path with auto-controlled gain. An uneven-step time-to-digital TDC is implemented for low-power and small chip area consideration. The proposed ADPLL has been fabricated in a 0.18 μm CMOS technology. With less than 5 us locking time, the measured rms jitter from a 2.49 GHz carrier is about 1.93 ps. The whole ADPLL occupies a chip area of 1.8 mm² and dissipates 10.35 mA from a 1.8 V supply.

12-5 15:30-15:42

A Cint-Less Type-II PLL with Delta-Sigma DAC Based Frequency Acquisition and Reduced Quantization Noise

Zhuo Zhang, Xican Chen, Woogeun Rhee, Zhihua Wang (Tsinghua University, China)

Abstract: This paper describes a type-II PLL architecture in which a large-area integral-path capacitor (Cint) is replaced with a delta-sigma DAC based frequency acquisition circuit. The proposed voltage-mode acquisition method provides inherent quantization noise suppression by the PLL loop filter. A 1.43-to-2.41GHz Cint-less PLL is implemented in 0.18um CMOS where the DAC area is <10% of the total area. The PLL achieves the in-band phase noise of -90dBc/Hz and the reference spur of -55dBc with 500kHz loop bandwidth.

12-6 15:42-15:55

Delay-Line Based Fast-Locking All-Digital Pulsewidth- Control Circuit with Programmable Duty Cycle

Jun-Ren Su, Te-Wen Liao, Chung-Chih Hung (National Chiao Tung University, Taiwan)

Abstract: This paper proposes an all-digital fast-locking pulsewidth-control circuit with programmable duty-cycle. In comparison with prior art, our use of two delay lines and a time-to-digital detector allows the pulsewidth-control circuit to operate over a wide frequency range with fewer delay cells, while maintaining the same level of accuracy. This study presents a new duty-cycle setting circuit that calculates the desired output duty cycle without the need for a look-up table. The circuit was fabricated under the TSMC 0.18-um CMOS process. Results show that the proposed circuit performs well for an input operating frequency ranging from 200 to 600MHz, and an input duty cycle ranging from 30 to 70%. It achieves a programmable output duty cycle ranging from 31.25 to 68.75% in increments of 6.25%.

Session 13 SSD Memory and High Frequency Analog

Time: 16:10 - 18:02

Room: 301

Co-Chairs : Yasuhiro Sugimoto (Cyuo University)

Atsushi Kawasumi (Toshiba)

13-1 16:10 – 16:35

VSET/RESET and VPGM Generator Without Boosting Dead Time for 3D-ReRAM and NAND Flash Hybrid Solid-State Drives

Kousuke Miyaji, Koh Johguchi (Chuo University, Japan), Kazuhide Higuchi (University of Tokyo, Japan), Ken Takeuchi (Chuo University, Japan)

Abstract: A single-inductor, dual-output, parallel-boosting (SIDOPB) boost converter which simultaneously outputs 3V for ReRAM program Vset/reset, 20V for NAND flash program Vpgm, is proposed for a hybrid ReRAM and NAND flash 3D-integrated solid-state drive (SSD). Simultaneous boosting of two programming voltages is experimentally demonstrated without boosting dead time for the first time. Interference between ReRAM and NAND boosters is suppressed by the inductor design. There is no additional power increase or the performance degradation compared with the conventional boost converter using double-coil SSD. The area is reduced by 15%.

13-2 16:35 – 17:00

An Integrated Variable Positive/Negative Temperature Coefficient Read Reference Generator for MLC PCM/NAND Hybrid 3D SSD

Kousuke Miyaji, Koh Johguchi (Chuo University, Japan), Kazuhide Higuchi (University of Tokyo, Japan), Ken Takeuchi (Chuo University, Japan)

Abstract: An integrated variable temperature coefficient (TC) reference generator for MLC PCM/NAND flash memory hybrid 3D SSD is proposed and demonstrated by 0.18um CMOS process. The proposed generator outputs both positive and negative TC reference current and voltage for PCM and NAND, respectively. TC can be varied from -5.47 to 5.74mV/K. Output level is also independently controlled from the TC control to enable a compensation of characteristics changes due to the program/erase cycling as wells as the process variations of the memory devices. The size of the reference generator is 0.195mm2. The power consumption is 0.68mW at 120degC, 2.3V output.

13-3 17:00 – 17:25

A 5.8GHz Digital Arbitrary Phase-Setting Type II PLL in 65nm CMOS with 2.25° Resolution

Li Li (University of Michigan, United States), Mark Ferriss (IBM T. J. Watson Research Center, U.S.A), Michael Flynn (University of Michigan, US.A)

Abstract: A fully-integrated 5.8GHz PLL modulator implemented in 65nm CMOS achieves digitally-controlled arbitrary phase generation. The PLL consists of a Type II fractional-N PLL with a 1-bit TDC as its PFD. Digital phase setting, which operates by adding a proportional signal to the PFD output, is incorporated in the PLL. The prototype achieves an average phase resolution of 2.25° and a phase range of more than 720°. The entire PLL and output buffer consumes 11mW.

13-4 17:25-17:50

A 0.5V GFSK 200uW Limiter/Demodulator with Bulk-Driven Technique for Low-IF Bluetooth

Chang Ming Lai, Meng Hung Shen, Yi Shuan Wu, Po-Chiun Huang (National Tsing Hua university, Taiwan)

Abstract: This paper presents a low-voltage IF processor including a limiter and a DLL-based demodulator for Bluetooth receiver. The limiter amplifies the received IF signals with constant envelope. The demodulator detects and manipulates the edges of the IF signal. To achieve 0.5V operation the bulk-driven technique are extensively used in amplifier design nd more digital-like operations are used in demodulator. With the IF frequency of 3MHz, the power consumption of the limiter and demodulator is only 200μ┬W. The core area is 0.36 mm² using a standard 0.18-μm CMOS process. Measurement result shows that a 18.7-dB input signal-to-noise ratio is obtained for a 0.1% bit error rate.

13-5 17:50-18:02

Wireless Wafer Probing for on-Chip Analog Voltage Measurement

Dae Young Lee, David Wentzloff, John Hayes (University of Michigan, U.S.A)

Abstract: This paper demonstrates a method for wirelessly measuring analog voltage on DUTs. This technique can be used for test structure characterization. The proposed voltage-to-time converter enables analog voltage values to be wirelessly delivered through capacitive coupling. A dual-slope architecture is adopted to mitigate the effects of on-chip R and C variation, and an UWB pulse generator is used to relay accurate timing to the ATE with low-power consumption. A prototype, fabricated in 0.13 um CMOS achieves 8-bit resolution with 1 mV measurement steps. The total area of the on-chip wireless voltage measurement circuit is 0.013 mm^2 excluding wireless pads.

Session14 Ultra Low-Power Circuits for Emerging Communication Systems

Time: 16:10 - 18:15

Room: 401

Co-Chairs : Jerald Yoo (Masdar Institute of Science and Technology)

Seungjun Lee (Ewha Womans University)

14-1 16:10 – 16:35

Photovoltaic-Assisted CMOS Rectifier Circuit for Synergistic Energy Harvesting from Ambient Radio Wave

Koji Kotani, Takumi Bando, Yuki Sasaki (Tohoku University, Japan)

Abstract: We realized efficient energy harvesting from ambient radio waves using a photovoltaic (PV) assisted CMOS rectifier. It operates truly synergistically, where a pn-junction diode acting as a PV cell converts light energy to a dc bias voltage, which compensates Vth of the MOSFETs and enhances the RF-radio-wave-to-DC power conversion efficiency (PCE) of the rectifier even under the very small input power condition. Under the room light condition, PCE of more than 20% was achieved at RF input power, frequency and output load of -20 dBm, 920 MHz and 47 kOhm, respectively, which is twice as large as the conventional rectifier without PV assistance.

14-2 16:35 – 17:00

A 45uW Injection-Locked FSK Wake-Up Receiver for Crystal-Less Wireless Body-Area-Network

Joonsung Bae, Hoi-Jun Yoo (KAIST, Korea)

Abstract:: A dedicated ultra-low power fully integrated FSK wake-up receiver (WuRx) for wireless body area network (WBAN) is implemented in 0.18um CMOS technology with 0.7V supply. An injection-locking digitally-controlled oscillator (IL-DCO) enables power-efficient front end amplification, and auto-calibration of DCO by successive approximation resister (SAR) algorithm. The fabricated 1mm2 single chip WuRx consumes 45uW with a data rate of 312kb/s, providing an 80MHz reference frequency with 0.25% stability to the main transceiver for crystal-less WBAN sensor nodes.

14-3 17:00 – 17:25

A 2.4/5.8 GHz 10 μW Wake-Up Receiver with -65/-50 dBm Sensitivity Using Direct Active RF Detection

Kuang-Wei Cheng (National Cheng Kung University, Taiwan), Xin Liu, Minkyu Je (Institute of Microelectronics, Singapore)

Abstract: This paper presents a fully integrated wake-up receiver (WuRx) with direct active RF detection. The RF front-end features a high-sensitivity RF detector embedded with input matching network, obviating the need of RF amplification and LO generation for frequency downconversion. This complete receiver contains an RF detector, IF amplifiers, and a continuous-time $\Sigma\Delta$ ADC to provide inherent anti-alias filtering, which simplifies the overall design in 0.18-μm CMOS process. It achieves a sensitivity of -65 dBm for data rate of 100 kbps, operating in 2.4 GHz ISM band with only 10 μW. By adjusting the input matching, it can also operate for 5.8 GHz band, providing -50 dBm sensitivity without additional power consumption.

14-4 17:25-17:50

An Asymmetrical QPSK/OOK Transceiver SoC and 15:1 JPEG Encoder IC for Multifunction Wireless Capsule Endoscopy

Yuan Gao, San Jeow Cheng, Wei Da Toh, Yuen Sam Kwok, Kay-Chuan Benny Tan, Xi Chen, Wai-Meng Mok, Htun Htun Win, Bin Zhao, Shengxi Diao, Cabuk Alper, Yuanjin Zheng, Sumei Sun, Minkyu Je (Agency for Science, Technology and Research, Singapore), Chun-Huat Heng (National University of Singapore, Singapore)

Abstract: A chipset including a low power asymmetrical QPSK/OOK transceiver SoC and a 15:1 JPEG image encoder IC is presented for wireless capsule endoscopy. The proposed asymmetrical bi-directional telemetry link supports high-data-rate image transmission with QPSK modulation and low-data-rate actuator control data reception with OOK modulation. To transmit high-quality images with high spectral efficiency, a low power JPEG encoder with compression ratio as high as 15:1 is employed to compress raw image data with subsampling technique in YUV color plane. Implemented in 0.18-μm CMOS, the QPSK TX consumes 5 mW at ? dBm of output power with 3-Mb/s data rate while the OOK RX achieves ?0 dBm of sensitivity at 500-kb/s data rate with 6-mW power consumption. A prototype capsule system has been implemented for wireless endoscopy using the developed chipset. With duty cycling, the average power consumption of TX is 2.5 mW when transmitting at 3-fps frame rate.

14-5 17:50-18:02

A QPSK/16-QAM OFDM-Based 29.1Mbps LINC Transmitter for Body Channel Communication

Ping-Yuan Tsai, Shu-Yu Hsu, Jen-Shin Chang (National Chiao-Tung University, Taiwan), Tsan-Wen Chen (MediaTek Inc., Taiwan), Chen-Yi Lee (National Chiao-Tung University, Taiwan)

Abstract: This paper proposed a high speed Body Channel Communication transmitter, adopting the OFDM modulation and uneven multi-level LINC technique to reduce the power and complexity of the front-end circuit. The phase modulator in the Linear amplification with Nonlinear Component (LINC) transmitter uses not only clock-gating scheme but also the glitch free protection. A detection and calibration DSP are also integrated to solve the LINC branch mismatch problem. Finally the capacitive sensing circuit provides the information of the connectivity between pastes and human. The chip is implemented by 90nm CMOS process, with die area 1.3mm2. The maximum data rate could achieve 29.1Mbps and the total power is 1.925mW, resulting in 0.07nJ/b transmission energy and 2.92 bps/Hz spectral efficiency.

14-6 18:02-18:15

Continuous-Time High-Precision IR-UWB Ranging-System in 90 nm CMOS

Shanthi Sudalaiyandi, Håkon André Hjortland, Tuan-Anh Vu, Øivind Næss,
Tor Sverre Lande

Shanthi Sudalaiyandi, Håkon André Hjortland, Tuan-Anh Vu, Øivind Næss, Tor Sverre Lande (University of Oslo, Norway)

Abstract: Precision ranging is a key factor for localization in wireless sensor networks. But most reported ranging solutions are limited by clock frequency or clock synchronization. With the combination of continuous-time binary value (CTBV) technique and the impulse-radio ultra-wideband (IR-UWB) technology, we have a promising approach towards high precision positioning combined with communication. In this paper, we have presented a UWB communication solution with embedded ranging by measuring the symbol round trip time without a common reference clock. A first working clockless UWB ranging transceiver realized in 90 nm CMOS technology with fully integrated digital symbol detection including a running cross-correlator is implemented. Preliminary measured results shows that two transceivers in a master-slave configuration can estimate distance with centimeter precision (≒1.4 cm).

Session15 VCO & PLL

Time: 16:10 - 18:15

Room: 402

Co-Chairs : Julien Ryckaert (IMEC)

Baoyong Chi (Tsihghhua University)

15-1 16:10 – 16:35

A 0.38 mm², 10MHz-6.6 GHz Quadrature Frequency Synthesizer Using Fractional-N Injection-Locked Technique

Wei Deng, Ahmed Musa, Kenichi Okada, Akira Matsuzawa (Tokyo Institute of Technology, Japan)

Abstract: This paper presents an area- and power-efficient delta-sigma frequency synthesizer with a quadrature phase output using a fractional-N injection-locked technique. A digital calibration scheme is proposed to compensate for the PVT variations. Implemented in a 65nm CMOS process, this work demonstrates 10 MHz to 6.6 GHz continuous frequency coverage with quadrature output, while only occupies a small area of 0.38 mm² and consumes 16-26 mW depending on output frequency. The normalized phase noise achieves -135.3 dBc/Hz at 3 MHz offset, and -95.1 dBc/Hz in-band phase noise at 10 kHz offset, from a 1.7GHz carrier frequency.

15-2 16:35 – 17:00

A 0.5-V 5.5-GHz Class-C-VCO-Based PLL with Ultra-Low-Power ILFD in 65 nm CMOS

Sho Ikeda, Tatsuya Kamimura, Sangyeop Lee, Norifumi Kanemaru, Hiroyuki Ito, Noboru Ishihara, Kazuya Masu (Tokyo Institute of Technology, Japan)

Abstract: In this paper, a ultra-low-power 5.5-GHz PLL is proposed, which employs the new divide-by-4 injection-locked frequency divider (ILFD) and a class-C VCO for operation under a power supply of 0.5V. A forward-body-biasing (FBB) technique can decrease threshold voltage of MOS transistors, which can improve operation frequency and can widen the lock range of the IFLD. The double-switch injection technique is also proposed to widen the lock range of the ILFD. The proposed PLL was fabricated in 65nm CMOS. The circuit totally consumes 1.6mW under the power supply of 0.5V. With a 34.6-MHz reference, it shows an 1-MHz-offset phase noise of 􀀀105 dBc/Hz and a reference spur level lower than 􀀀65 dBc at 5.5 GHz.

15-3 17:00 – 17:25

An Energy-Efficient 2.4-GHz PSK/16-QAM Transmitter

Chun-Yu Lin (National Taiwan University, Taiwan), Yao-Hong Liu (IMEC - Holst Centre, Netherlands), Chang-Tsung Fu, Hasnain Lakdawala (}Intel Corporation, U.S.A), Tsung-Hsien Lin (National Taiwan University, Taiwan)

Abstract: A 2.4-GHz energy-efficient transmitter (TX) which supports multiple modulation schemes is reported. The proposed TX is based on the phase-selector architecture, where the modulation signal is generated by interpolating among quadrature phases at RF. This TX demonstrates the capability of supporting various PSK (OQPSK, HS-OQPSK, and 8-PSK) and the 16-QAM modulations. Fabricated in a 90-nm CMOS process, the TX consumes 8.8 mW and 13.7 mW at PSK and QAM modes, respectively. The maximum data rate is 105-Mbps under -3 dBm output power and 10.6 % EVM.

15-4 17:25-17:50

Heterogeneous Coupled Ring Oscillator Arrays for Reduced Phase Noise at Lower Power Consumption

Prashant Dubey (Synopsys India Pvt. Ltd., India), Didier Belot (STMicroelectronics, France), Shouri Chatterjee (Indian Institute of Technology Delhi, India)

Abstract: Phase noise in coupled-oscillator arrays of singleended inverter-based ring-oscillators has been analyzed using a time-domain delay-based model for injection locking. This paper demonstrates a heterogeneous coupled-oscillator array (multiple frequency oscillators coupled to each other) which can decrease phase noise, with an improvement in power consumption, viz. for a 15 dB reduction in phase noise, we increase power consumption by only 12 dB. An oscillator running at 2.56 GHz coupled with an oscillator array of 36 coupled oscillators running at 1.28 GHz, was measured to have a phase noise of -103 dBc/Hz at a 1 MHz offset from the center frequency of 2.56 GHz, with a total power consumption of 3.7 mW.

15-5 17:50-18:02

A Low Voltage Sub 300uW 2.5GHz Current Reuse VCO

Mazhareddin Taghivand (Stanford University, Qualcomm Atheros, U.S.A), Mohammad Mahdi Ghahramani , Michael Flynn (University of Michigan, U.S.A)

Abstract: The two-transistor CMOS current reuse VCO is modified with the addition of an ac-coupling capacitor to reduce the supply voltage and achieve good phase noise with very low power consumption. A 2.17-2.9GHz prototype VCO operates with a supply voltage as low as 0.6V. At 2.53GHz, with a 0.7V supply and a 185μW power consumption, the measured phase noise at 3MHz offset is -122.6dBc/Hz and varies by only 2.2dB over a temperature range from -30 to 120°C. For a 0.85V supply, phase noise is improved to -126.1dBc/Hz with a 280μW power consumption which corresponds to a Figure of Merit (FoM) of 190.2dB. This is the lowest reported power consumption and supply voltage for any current reuse VCO. Fabricated in 65nm CMOS, the prototype occupies 0.13mm².

15-6 18:02-18:15

4 GHz Locking Range and 0.19 pJ Low-Energy Differential Dual-Modulus 10/11 Prescaler

Takeshi Mitsunaka, Masafumi Yamanoue, Kunihiko Iizuka (SHARP Corporation, Japan), Minoru Fujishima (Hiroshima University, Japan)

Abstract: We present a differential dual-modulus prescaler based on an injection-locked frequency divider (ILFD) for a satellite low noise block (LNB) down converter. Three stage differential latches using ILFD and a cascaded differential divider can achieve divide-by-10/11 operations with a lock range of 2.1 GHz - 10 GHz at a supply voltage of 1.4 V and an operating frequency range of 2.1 GHz - 6.1 GHz at a supply voltage of 1 V. At our target frequency, 5 GHz, a minimum energy of 0.19 pJ (=mW/GHz) at the maximum input frequency can be achieved. Our proposed circuit is fabricated by a 130 nm CMOS process, and the prototype chip core area is 40 um X 20 um2.

Session16 Low-Power SoCs & Circuits

Time: 16:10 - 18:15

Room: 403

Co-Chairs : Zhiyi Yu (Fudan University)

Chenyi Lee (National Chiaotung University)

16-1 16:10 – 16:35

Real-Time Instruction-Cycle-Based Dynamic Voltage Scaling (iDVS) Power Management for Low-Power Digital Signal Processor (DSP) with 53% Energy Savings

Shen-Yu Peng, Yu-Huei Lee, Chun-Hsien Wu, Tzu-Chi Huang, Ke-Horng Chen (National Chiao Tung University, Taiwan), Ying-Hsi Lin, Chao-Cheng Lee, Chen-Chih Huang, Ching-Yuan Yeh (Realtek Semiconductor Corporation, Taiwan), Yu-Wen Chen (Vanguard International Semiconductor Corp., Taiwan), Chao-Chiun Liang, Chang-An Ho, Tun-Hao Yu (National Chiao Tung University, Taiwan)

Abstract: this paper presents an instruction-cycle-based dynamic voltage scaling (iDVS) power management strategy for a low-power processor design. The iDVS technique is fully compatible with conventional DVS scheduler algorithms. Furthermore, an additional iDVS design flow embedded in the standard cell lib flow is proposed to implement the iDVS-based DSP. In addition, the fast-response bidirectional asynchronous wave-pipeline (BAWP) digital low-dropout (LDO) regulator is also presented to improve the iDVS performance. The iDVS-based DSP chip implemented in an HH-NEC 0.18μm standard CMOS process demonstrates 53% energy savings over that without the iDVS technique.

16-2 16:35 – 17:00

Ultra-Low-Energy Near-Threshold Biomedical Signal Processor for Versatile Wireless Health Monitoring

Xin Liu, Jun Zhou, Xiongfei Liao, Chao Wang, Jianwen Luo, Mohammad Madihian, Minkyu Je (Agency for Science, Technology and Research, Singapore)

Abstract: In this paper, an ultra-low-energy biomedical signal processor (BSP) is proposed for wireless multi-channel physiological signal monitoring. This BSP integrates a RISC core and application-specific hardware accelerators (ASHAs) to achieve ultra low power consumption while meeting required performance. Various low power design techniques from system to circuit levels are applied, including event-driven signal processing, dynamic clock management, near-threshold operation, glitch-free clock generation, fine-grain clock gating, and ultra-low-voltage level shifting. The BSP can operate with supply from 1.8V down to 0.5V. With integrated ECG ASHAs based on the discrete wavelet transform, its overall energy consumption is 20.4pJ/cycle at 0.5V and 10MHz when performing a real-time wireless ECG monitoring.

16-3 17:00 – 17:25

Performance and Side-Channel Attack Analysis of a Self Synchronous Montgomery Multiplier Processing Element for RSA in 40nm CMOS

Benjamin Devlin (University of Tokyo, Japan), Hiroshi Ueki, Shintaro Mori, Shigenori Miyauchi (Renesas Electronics Corporation, Japan), Makoto Ikeda, Kunihiro Asada (University of Tokyo, Japan)

Abstract: We propose a Montgomery multiplier composed of gate-level self synchronous processing elements (SS-PE) that can be used to create scalable-length modular multipliers with no broadcast signals for high throughput. A 40nm test circuit shows the SS-PE operates from 0.4V to 1.3V at 20C without tuning, with 2.1 Gb/s data-throughput, 476ps delay at 1.1V, and energy per operation of 322fJ/op at 1.1V and 1.40fJ/op with voltage scaling to 0.4V. A 8-bit RSA is implemented using SS-PEs, and shows 186Mb/s and 130ns data-throughput and time respectively for the average case of decryption. Side-channel attacks using simple power analysis, differential power analysis, and high order differential power analysis show secure operation with no information leakage after 50,000 measurements.

16-4 17:25-17:50

A Body Bias Generator Compatible with Cell-Based Design Flow for Within-Die Variability Compensation

Norihiro Kamae, Akira Tsuchiya, Hidetoshi Onodera (Kyoto University, Japan)

Abstract: A body bias generator (BBG) for fine-grain body biasing (FGBB) compatible with cell-based design flow is proposed. The FGBB is effective to reduce variability and power consumption in a system-on-chip. Since FGBB needs a number of BBGs, automated design flow of BBGs is required. This paper proposes a design of the BBG to implement the BBG in a cell-based design flow. Circuit configuration of the BBG enables wide range of the supply voltage from 0.6V to 1.2V. We fabricated the BBG in a 65nm CMOS process to control 0.1mm2 of core circuit with the area overhead of 1.4%.

16-5 17:50-18:15

Self-Test Methodology and Structures for Pre-Bond TSV Testing in 3D-IC System

Chao Wang, Jun Zhou, Bin Zhao, Xin Liu, Philippe Royannez, Minkyu Je (Agency for Science, Technology and Research, Singapore)

Abstract: This paper presents a self-test methodology and test structures for testing Through Silicon Vias (TSVs) in 3D-IC system prior to stacking in order to improve overall yield. A Scan Switch Network (SSN) architecture is proposed to perform pre-bond TSV scan testing. In the SSN, novel self-test structures are proposed and integrated to detect TSV defects by stuck-at-fault and delay-based tests. By exploiting the inherent delay characteristics of TSV, the variation of TSV-to-substrate resistance caused by TSV defects can be mapped to a path delay change and detected. Compared with prior works, the proposed test architecture addresses pre-bond TSV testing under an integrated test solution with low overhead. Test chip measurement and analysis are presented to verify the proposed self-test methodology and structures.