Call for Papers

IEEE Asian Solid-State Circuits Conference

A-SSCC 2015

Location: Xia'men International Conference Center (XICC), China

Date: 9 – 11 November 2015

Sponsored by IEEE SSCS, IEEE Region-10 SSCS Chapters

http://www.asscc.org

http://sscs.ieee.org

Conference Theme — Securing the Society with Silicon Systems

As our society depends more and more on Silicon Systems, we need to be seriously concerned about the reliability of Silicon Systems, considering temporal errors induced by variability, soft errors, and aging of transistors such as BTI. Systems need to cope with such effects through error correction, early possible failure detection, and self-healing of aging. Also, silicon systems are keys to preventing un-necessary data leakage from the clouds by breaking ciphers, and more over, silicon systems should be reliable and safe against tampering by power attacks, electro-magnetic probing, and so on. Silicon systems should be trustworthy against hardware Trojan insertion as well.

The IEEE A-SSCC 2015 (Asian Solid-State Circuits Conference) is an international forum for presenting the most updated and advanced chips and circuit designs in solid-state and semiconductor fields. The conference is supported by the IEEE Solid-State Circuits Society and will be held in Asia. Further details on the conference and paper submission guidelines and templates will be available at the A-SSCC official website http://www.asscc.org/ around the beginning of April, 2015.

Paper Submission

Prospective authors are invited to submit full-length, four-page manuscripts, including figures, tables and references, to the official A-SSCC 2015 website. All papers will be handled and reviewed electronically. Papers are solicited in the following categories:

Regular Session

1. **Analog Circuits & Systems:** Amplifiers, comparators, switch capacitor circuits, continuous-time & discrete-time filters, voltage/current references; DC-DC converters, power-control circuits; IF/baseband analog circuits, AGC/VGA; display driver circuits; non-linear analog circuits.
2. **Data Converters**: Nyquist-rate and oversampling A/D and D/A converters, sub-circuits for data converters including sample-and-hold circuits, calibration circuits.
3. **Digital Circuits & Systems:** Design, fabrication, and test of digital VLSI systems; high-speed low-power digital circuits, power-reduction and management methods for digital VLSI, ultra-low-voltage and sub-threshold logic design; leakage reduction techniques; clock distribution, I/O circuits, reconfigurable logic-array circuits; supply/substrate noise measurement and cancellation for digital VLSI, variation and fault-tolerant circuits.
4. **SoC & Signal Processing Systems:** System-on-chip, microprocessors, network processors, baseband communication processing system & architectures, low-power signal-processing systems; multimedia processors including video, image, audio and voice processing systems; cryptographic and security-processing circuits and systems; bio-medical/neural signal processors.
5. **RF:** Receivers/transmitters/transceivers for wireless systems; narrowband RF, ultra-wideband and millimeter-wave circuits; circuits and building-blocks including RF front-end, LNA, mixer, power amplifiers, VCOs, frequency synthesizers, RF filters, RF switches, power detectors, active antennas.
6. **Wireline & Mixed-Signal Circuits:** Receivers/transmitters/transceivers for wireline systems including (but not limited to) LAN, WAN, FDDI, Ethernet, token-ring, fiber channel, SONET, SDH, PON, ATM, ISDN, xDSL, cable-modem; optical/electrical data links and backplane transceivers; power-line communication; clock generation circuits, PLL, DLL, spread-spectrum clock generation.
7. **Emerging Technologies and Applications:** Advanced digital and analog system designs for emerging devices including molecular-, organic-, and nano-electronics, flexible substrates and printable electronics; 3D-integration and packaging technologies; compound-semiconductor, superconductive, and micro-photonic technologies and circuits; energy harvesting; medical/bio-electronics/bio-inspired chip design and silicon systems for deep-learning; advanced memory technologies; spintronics; quantum storage.
8. **Memory:** Static, dynamic, non-volatile, read-only memory; magnetic, ferro-electric, nano-crystal, phase change, and 3D memory designs and architectures; data storage and multi-bit-cell-based memory design; embedded memory architecture, cache-memory system, multi-port memory, and CAM design; yield-enhancement redundancy and ECC techniques; memory testing and built-in self-test.

Special Session

1. **Industry Program:** This special category accepts only papers based on state-of-the-art products. Strong emphasis on systems realized by silicon chips is encouraged. The paper may cover specifications and application systems, achievements by chips, chip photos, chip architecture from software to circuits (not necessarily very original, significant improvement is fine), live demo if any, characterization results, and packaging/testing results.
2. **Student Design Contest:** A student design contest is held among **the accepted papers** with system prototypes or measurement results of which operations can be demonstrated on-site. Refer to the web for further information.

Papers related to securing silicon systems are highly solicited. Papers on low-power and/or low-voltage approaches, signal integrity, noise, test, and manufacturability for all the above categories are welcomed. Measurement results are highly recommended, especially for analog, and RF categories. Design methodologies for SiP, and SoC are included in the scope of the conference; the papers only describing CAD tools and CAD algorithms are not considered. Authors must follow detailed instructions provided within the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. The technical content beyond the abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Conference. Extended versions of selected papers from the Conference will be published in a **Special Issue of the IEEE Journal of Solid-State Circuits**.

Important dates

June 22, 2015, 20:00 (GMT) — **Paper submission deadline**

Aug. 7, 2015 — **Acceptance notification**

September 11, 2015 — **Deadline for final paper submission**

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